

ES 154 Assignment #5

Due: 2:00pm, November 5th, 2009

Instructor: Donhee Ham

Teaching Fellows: Sinbae Kim & Nan Sun

Problem 1 (30 pt)

Check your results of Problem 3, Assignment #3 with SPICE. More specifically, using SPICE, simulate the input-output transfer characteristic and low-frequency small signal gain of the circuit in the problem and compare them to the results you calculated earlier. Do this for both $V_{CC} = 1.8V$ and $V_{CC} = 10V$.

Problem 2 (40 pt)

Calculate the dc collector currents in transistors Q1 and Q2 for the Darlington-pair circuit of Fig. 1, approximating $V_{BE(on)} \approx 0.6 V$. Calculate the input resistance and voltage gain of the circuit, using the simple small signal model where you may neglect r_o . Check your answer with SPICE, and also use SPICE to determine the output resistance of the circuit.

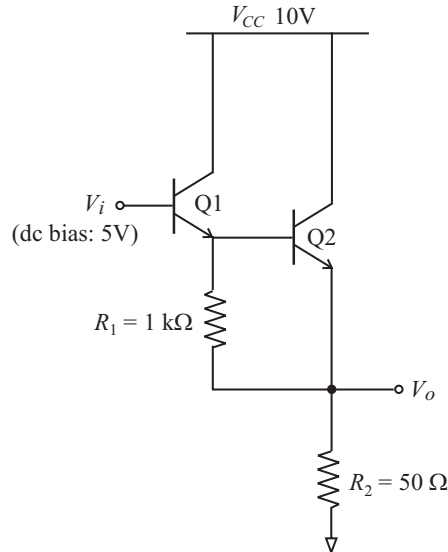


Figure 1: For the *npn* transistors, use: $\beta = 200$; $I_s = 5 \times 10^{-15} A$; $V_{CE,sat} = 0.2V$; $V_A = \infty$.

Problem 3 (60 pt)

Figure 2 shows a common-source amplifier. The NMOSFET has the following physical parameters: $t_{ox} = 15 \text{ nm}$; $\mu_n = 550 \text{ cm}^2/V \cdot s$; $V_{th} = 0.7 \text{ V}$; $V_A = \infty$.

(a) Plot the V_i - V_o transfer function. You should specify the numerical value for V_i at which the NMOSFET enters the triode region from the pinch-off region (Calculation of this value involves a quadratic equation).

(b) Calculate the value of V_i at which $V_o = 1 \text{ V}$.

(c) Calculate the bias values of V_i and V_o (in the pinch-off region) where the small-signal gain G becomes unity.

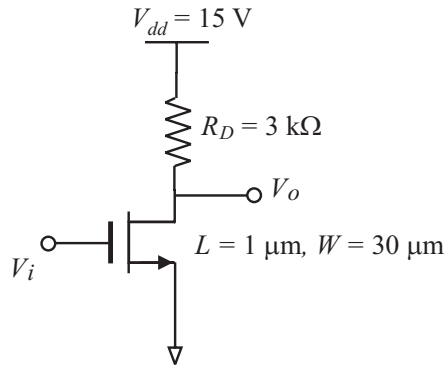


Figure 2: Common source amplifier.

(d) Calculate the bias values of V_i and V_o (in the triode-region) where the small-signal gain G becomes unity.

(e) Suppose the gate is biased at 1.47 V (this puts the transistor in the pinch-off region). Calculate the drain current I_D , transconductance g_m , and small signal gain G .

(f) What is the maximum small signal gain of this circuit? (At what gate bias is the maximum small signal gain obtained?)

(g) Use SPICE to check your results in (a) through (f) above. You can use (and modify, if needs be) the following SPICE code:

(h) Using SPICE, observe how the V_i - V_o transfer function is altered as you change V_A from ∞ to 100 V. Explain why. By measuring the slope of the transfer curve at $V_i=1.47$ V in SPICE, obtain the small signal gain G when $V_A = 100$ V. Compare this to the small signal gain you calculate using the small signal model ($V_A = 100$ V).

Problem 4 (40 pt)

(a) Show that the gate-source capacitance C_{gs} of a MOS transistor in the pinch-off region is given by

$$C_{gs} = \frac{2}{3}L_{eff}WC_{ox} \quad (1)$$

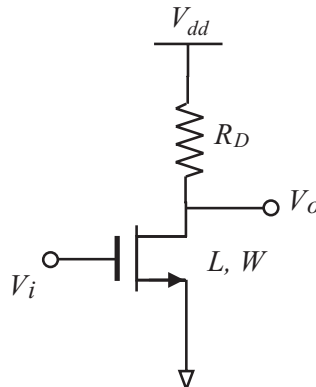


Figure 3: Common source amplifier.

(b) In class, we expressed the drain current I_D of an NMOSFET in the pinch-off region as

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L_{eff}} (V_{GS} - V_{th})^2 \quad (2)$$

Here L_{eff} is the effective channel length, which is a function of V_{DS} : if V_{DS} is increased, L_{eff} is decreased, thus, increasing I_D (Early effect in MOSFETs - or more accurately, channel length modulation effect). An alternative equation to capture this Early effect is

$$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}) \quad (3)$$

where $\lambda \equiv 1/V_A$ (we had a similar equation for BJT transistors - does this ring a bell?). Starting from this equation, express the V_i - V_o transfer characteristic of the common source amplifier of Fig. 3. From this transfer characteristic, show that the small signal gain $G = \partial V_o / \partial V_i$ for a given operating point is given by $-g_m(r_o || R_D)$, where $r_o = V_A / I_{D,0}$ where $I_{D,0}$ is the drain bias current at the given operating point.

Problem 5 (40 pt)

Fig. 4 shows a source follower circuit. As the input voltage at the gate is increased, the output voltage at the source is also increased, following the increase in the input voltage. This circuit is analogous to the emitter follower circuit using a BJT transistor we studied earlier. The NMOSFET used in Fig. 4 has the following physical parameters: $t_{ox}=15$ nm; $\mu_n=550$ cm²/V·s; $V_{th}=0.7$ V; $V_A = \infty$.

(a) Express V_o as a function of V_i , and plot the V_i - V_o transfer characteristic of the circuit. This involves solving a quadratic equation. Does the transistor ever enter the triode region?

(b) Derive the small signal gain G as a function of the gate bias V_i . You can obtain this by evaluating $\partial V_o / \partial V_i$ from the function you obtained in (a), or by working on the small signal model of the circuit, starting from the basic MOSFET small signal model.

(Note) In the circuit of Fig. 4, since the source of the MOSFET is not tied at ground, the threshold voltage V_{th} is not fixed at 0.7 V, but it varies with V_i due to the back-gate effect (or body effect), which we discussed in class. In (a) and (b), however, ignore this effect, and assume that V_{th} is constant, that is, 0.7 V.

(c) Using SPICE, check your results in (a) and (b). To be consistent with your calculation above, you should tell SPICE to ignore the back-gate effect. This can be done by stating “gamma=0.00001 (i.e., very small number)” in the line defining the nmos model, which starts with “.model...” (SPICE will have some difficulty with “gamma=0”).

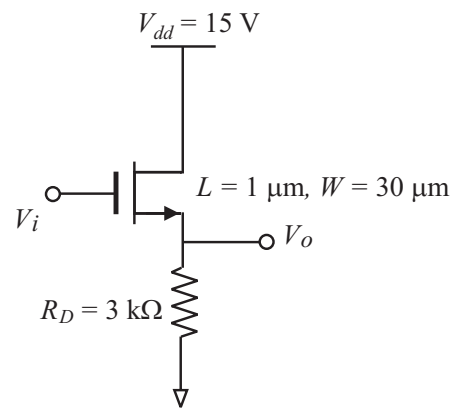


Figure 4: Source follower.