

ES 154 Assignment #6

Due: 2:00pm, November 12th, 2009

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Teaching Fellows: Sinbae Kim & Nan Sun

Problem 1 (40 pt)

Calculate the output resistance R_o of the Darlington-pair circuit of Fig. 1 as a function of I_{BIAS} . Do not neglect either $r_{o,1}$ (output resistance of transistor Q1) or $r_{o,2}$ (output resistance of transistor Q2) in this calculation. If the collector current of Q2 is 1 mA, what is R_o for $I_{BIAS} = 1$ mA? For $I_{BIAS}=0$?

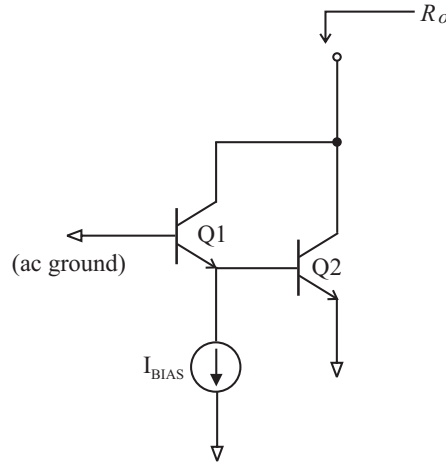


Figure 1: For the *npn* transistors, use: $\beta = 200$; $I_s = 5 \times 10^{-15}$ A.

Problem 2 (40 pt)

For the source follower of Fig. 2, assume $W/L=10$ and $\lambda = 0$ ($V_A = \infty$). Other MOSFET parameters are: $t_{ox}=25$ nm; $\mu_n=650$ cm²/V·s; $V_{th,0} = 0.7$ V (nominal threshold voltage); $N_A = 2 \times 10^{15}$ Atoms/cm³. For the intrinsic electron concentration, use $n_i = 1.5 \times 10^{10}$ Atoms/cm³. Find the dc output voltage V_O and the low-frequency small-signal gain under the following conditions:

- (a) Ignoring the back-gate effect (body effect) and with $R = \infty$.
- (b) Including the back-gate effect and with $R = \infty$.
- (c) Including the back-gate effect and with $R = 100$ k Ω .
- (d) Including the back-gate effect and with $R = 10$ k Ω .

Problem 3 (40 pt)

A BiCMOS (BJT and MOSFET are used together) amplifier is shown in Fig. 3. The bias voltage $V_{G,0}$ is adjusted to produce a dc output voltage of 2 V. Calculate the bias currents in both devices and calculate the low-frequency small-signal voltage gain of the amplifier. For the MOS transistor, assume $W = 10$ μ m, $L = 1$ μ m, $\mu_n C_{ox} = 200$ μ A/V², $V_{th,0} = 0.6$ V, $\gamma = 0.25$ V^{1/2}, $\phi_f = 0.3$ V, and $\lambda = 0$. For the bipolar transistor, assume $I_S = 10^{-16}$ A, $\beta = 100$, $r_b = 0$, and $V_A = \infty$. Use SPICE to check your result. Also use SPICE to compute the transfer characteristic of the amplifier.

Problem 4 (50 pt)

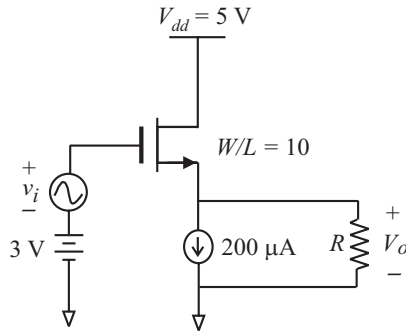


Figure 2: Source follower.

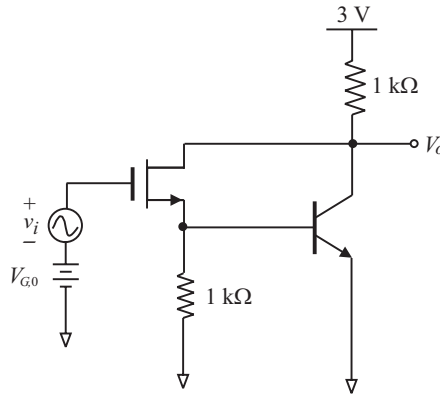


Figure 3: BiCMOS amplifier.

Plot the input-output (V_i - V_o) transfer characteristic of the circuit of Fig. 4. Calculate the small-signal gain, input resistance, and output resistance of the circuit when the dc bias of the base of transistor Q1 is 0V (ground). You may neglect r_o . Check your plot and calculations with SPICE.

Problem 5 (50 pt)

(a) Determine the differential-mode gain, common-mode gain, differential-mode input resistance, and common-mode input resistance (all at low frequencies) for the circuit of Fig. 5, which we discussed in class. Neglect r_b , r_o , and r_μ . Calculate the CMRR. Check with SPICE.

(b) Repeat (a) above, but with the addition of emitter-degeneration resistors of value 4 kΩ each [Fig. 6].

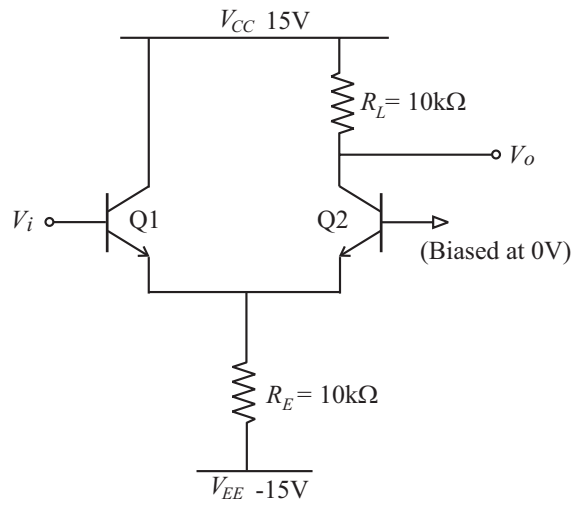


Figure 4: For the *npn* transistors, use: $\beta = 200$; $I_s = 5 \times 10^{-15} \text{ A}$; $V_{CE,sat} = 0.2 \text{ V}$; $V_A = \infty$.

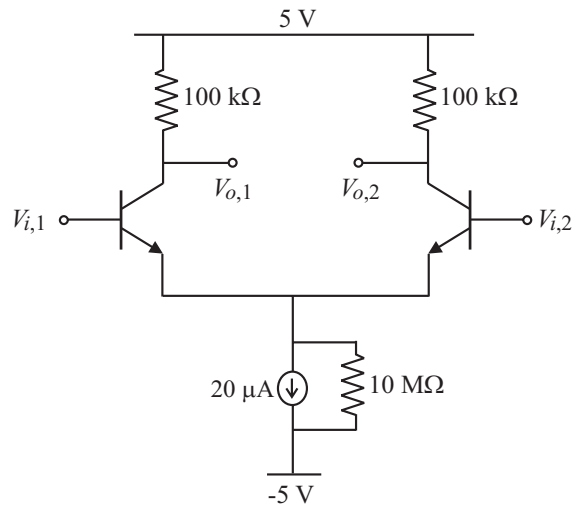


Figure 5: Emitter coupled differential amplifier.

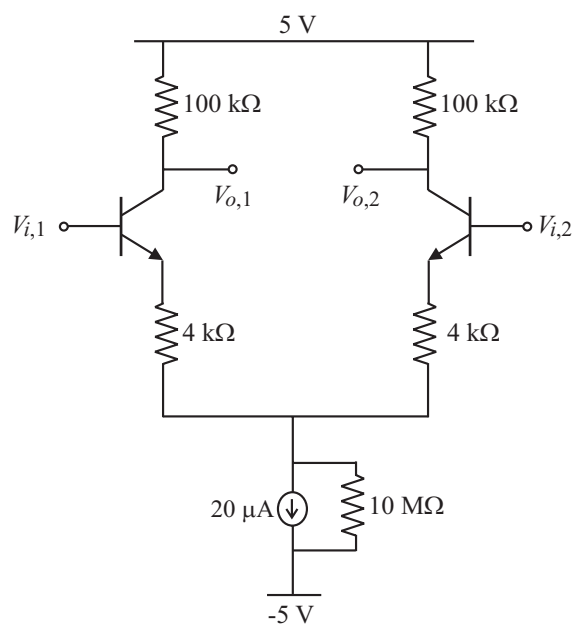


Figure 6: Emitter coupled differential amplifier with emitter degeneration.