

# ES 272: RF and High-Speed Integrated Circuits

## Spring 2009

School of Engineering and Applied Sciences  
Harvard University  
<http://www.seas.harvard.edu/courses/es272/>  
Time: 10:00 - 11:30, Tue/Thur.  
Place: Maxwell-Dworkin 223

### Teaching Staffs

Instructor: Donhee Ham (John L. Loeb Associate Professor of the Natural Sciences)  
— Maxwell-Dworkin Rm 131, 6-9451, donhee@seas.harvard.edu  
— (office hours) TBA

Teaching fellow: TBA  
— (office hours): TBA  
— (office): TBA

### Course Description

Design of RF and high-speed electronic circuits with special attentions to integrated circuits at both transistor and system levels. Topics (for details, see the following pages) include basic RF design concepts, wireless/wireline transceivers, active/passive devices, the physics of noise, amplifiers, low noise amplifiers, mixers, oscillators and phase noise, phase locked loops, frequency synthesizers, clock and data recoveries, and power amplifiers.

### Prerequisite

Transistor properties and operations (ES154 or equivalent), analog circuits (ES154 or equivalent), basic electromagnetism (Physics 11b or 15b or equivalent), basic differential equations (AM 21b or equivalent), and Fourier analysis (some part of AM 105a or ES 156 or equivalent).

### References

- RF Integrated Circuits
  1. Thomas H. Lee, *The Design of CMOS RF IC*, Cambridge University Press, 1998.
  2. Thomas H. Lee, *Planar microwave engineering*, Cambridge University Press, 2004.
  3. Razavi, *RF Microelectronics*, Prentice Hall, 1998.
- RF Electronics
  4. Clarke and Hess, *Communication Circuits: Analysis and Design*, Krieger Pub. Co., 1994.
  5. Hagen, *RF Electronics: Circuits and Applications*, Cambridge University Press, 1996.
- Analog IC
  6. Gray, Hurst, Lewis, and Meyer, *Analysis and Design of Analog IC's*, Wiley and Sons, 2001.
- Phase-locked loops
  7. Gardner, *Phaselock Techniques*, John Wiley & Sons, 1979.
- Electronics
  8. Horowitz and Hill, *The Art of Electronics*, 2nd edition, Cambridge University Press, 1989.

- Noise

9. Wax, *Selected Papers on Noise and Stochastic Processes*, Dover Publication, 1954.
10. Van Der Ziel, *Noise in Solid-State Devices and Circuits*, John Wiley and Sons, 1986.

### Grading

Grading will be based on homework & final project:

1. Homework (70%): Homework problems will be on analysis, simulation, and design of circuits, often using Cadence Spectre with BSIM MOS transistor models. Your solutions need not be wordy, but you should detail your reasoning. If we can't figure out what you did, your points will not be high.
2. Final project (30%): Phase-locked loop (PLL) frequency synthesizer design. The project details will be handed out after about 2/3 of lectures are finished.
3. Late grading policy: Homeworks are due Thursday mornings at the start of class, and will be graded by next Thursday. Late work will be reduced 25% per week. There is no exception to this rule, other than University-established emergency cases (a letter from authorized official is required).
4. Cooperation policy: Collaboration is allowed, but you should turn in your own homework — You can discuss any problem with other students taking the course, but final solutions should not be exchanged. You should make it sure that you understand the solution you turn in, and write up the solution in your own words. Basic guideline is not to take undue advantage of any other student.

### Estimated Schedule

NO.	SUBJECT
1	<i>Introduction</i>
2	<i>Amplifiers - Dynamic range</i>
3	<i>Amplifiers - Bandwidth</i>
4	<i>Cadence tutorial</i>
5	<i>Transmission lines</i>
6	<i>Distributed amplifiers</i>
7	<i>Noise</i>
8	<i>Amplifiers - Noise</i>
9	<i>Voltage references and current biasing</i>
10	<i>Mixers</i>
11	<i>Oscillators - I</i>
12	<i>Oscillators - II</i>
13	<i>Oscillators - III: frequency stability (phase noise)</i>

NO.	SUBJECT
14	<i>Phase locked loops (PLL) - I: fundamentals</i>
15	<i>Phase locked loops (PLL) - II: architectures and components</i>
16	<i>Phase locked loops (PLL) - III: architectures and components</i>
17	<i>PLL Frequency synthesizers - I</i>
18	<i>PLL Frequency synthesizers - II</i>
19	<i>PLL Frequency synthesizers - III</i>
20	<i>Wireless transceivers</i>
21	<i>Wireline communication transceivers and components - II</i>
22	<i>Clock and Data Recovery (CDR) - I</i>
23	<i>Clock and Data Recovery (CDR) - II</i>
24	<i>Power amplifiers (PA) - I</i>
25	<i>Power amplifiers (PA) - II</i>