

ES 272 Assignment #7

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(Problem 1) CMOS Quad Switching Mixer (50pt)

Figure 1(a) shows a differential CMOS passive switching mixer. Transistors M_1 and M_4 are driven by a sinusoidal local oscillator (LO) with a frequency of f_{LO} while transistors M_2 and M_3 are driven by the opposite phase of the same LO. Since the LO signal amplitude is typically substantially larger than the RF and IF signal amplitudes and the RF and IF signals have more or less the same dc values due to the circuit configuration, all of the MOS transistors operate between “off” and “on (triode)” regimes.

How the passive mixer multiplies the RF and LO signals to give the IF signal can be understood in the following way. When transistors M_1 and M_4 are on while M_2 and M_3 are off, $V_{IF} \equiv V_{+IF} - V_{-IF} \sim V_{+RF} - V_{-RF} \equiv V_{RF}$. Likewise when transistors M_2 and M_3 are on while M_1 and M_4 are off, $V_{IF} \sim -V_{RF}$. Therefore, $V_{IF}(t)$ is essentially $V_{RF}(t)$ multiplied by a periodic square pulse signal altering between 1 and -1 with a period of $1/f_{LO}$, where the periodic square pulse signal contains a $V_{LO}(t)$ component.

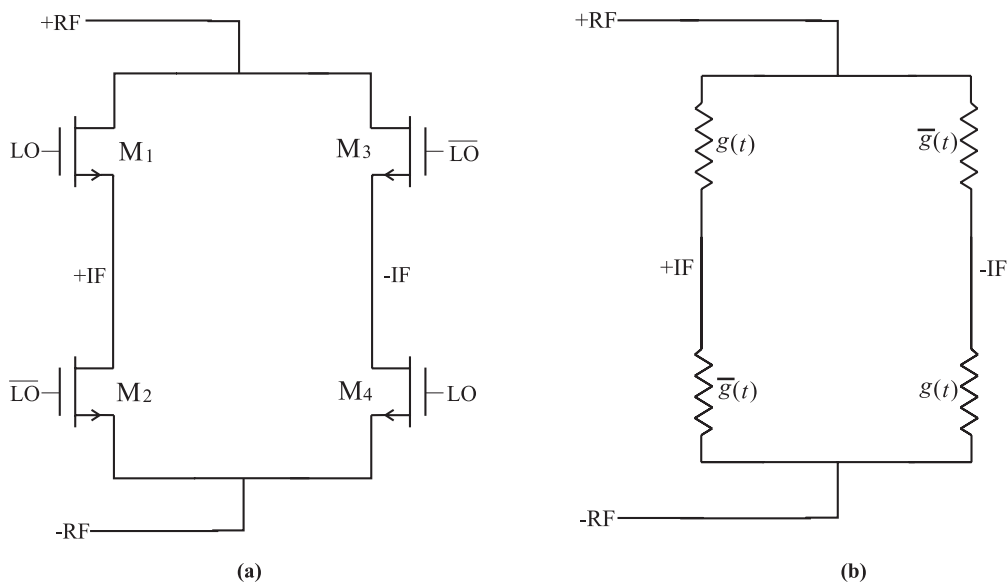


Figure 1: CMOS quad switching mixer

The above explanation, while capturing the essence, assumed that the $M_1 - M_4$ pair turns on immediately after $M_2 - M_3$ pair turns off and vice versa. This represents only one among the three possible switching modes, which will be explained shortly. Here in this problem, you are asked to calculate the voltage conversion gain ($\equiv |V_{IF}|/|V_{RF}|$) of the passive switching mixer in the various switching modes.

Figure 1(b) shows the equivalent switch model for the CMOS passive mixer. In the equivalent model, $g(t)$ represents the time-dependent (modulated by LO and RF signals) channel conductance of the MOS transistors, and when the transistor is in the triode-off regime, $g(t)$ is given by

$$g(t) = \mu_n C_{ox} \frac{W}{L} [V_{gs}(t) - V_{ds}(t) - V_{th}] \quad (1)$$

where μ_n , C_{ox} , L , and W are defined as usual, while $V_{gs}(t)$ is the gate-source voltage, $V_{ds}(t)$ is the drain-source voltage, and V_{th} is the threshold voltage of the MOS transistors. While V_{th} is time-dependent in general due to the body effect of the MOS transistors, here, it is regarded as constant to avoid complication. Since the LO signal amplitude is significantly larger than the RF signal amplitude, we can approximate the triode-regime channel conductance, $g(t)$, in the above as

$$g(t) \approx \mu_n C_{ox} \frac{W}{L} [V_{LO,ac}(t) + V_{LO,dc} - V_{RF,dc} - V_{th}] \quad (2)$$

Incorporating the transistors' off period, $g(t)$ can be more generally expressed as

$$g(t) \approx \begin{cases} \mu_n C_{ox} \frac{W}{L} [V_{LO,ac}(t) + V_{LO,dc} - V_{RF,dc} - V_{th}] & \text{(on \& triode: } g(t) > 0) \\ 0 & \text{(off)} \end{cases} \quad (3)$$

which is periodic in f_{LO} . In Fig. 1(b), $\bar{g}(t)$ is simply the 180° phase-shifted-version of $g(t)$.

From Fig. 1 and Eq. (3), we can see that the three switching modes briefly mentioned earlier are: *hard-switching*, *perfect-switching*, and *soft-switching*, where the criterion to determine the switching mode is given by

$$\Delta \equiv V_{LO,dc} - V_{RF,dc} - V_{th} \begin{cases} < 0 & \text{(hard-switching)} \\ = 0 & \text{(perfect-switching)} \\ > 0 & \text{(soft-switching)} \end{cases} \quad (4)$$

In the hard-switching mode, there is a period of time during which all transistors are off. In the soft-switching mode, there is a period of time during which all transistors are on. The perfect switching mode is at the borderline between the hard- and soft-switching modes, that is, $M_1 - M_4$ pair turns on immediately after $M_2 - M_3$ pair turns off and vice versa (this is the switching mode used in the second paragraph of this problem). By altering the *dc* biases of the LO and RF signals, one can go from one switching mode to another.

(a) Calculate the voltage conversion gain of the mixer in the perfect-switching mode ($\Delta = 0$). Is the voltage conversion gain a function of the LO signal amplitude in the perfect-switching mode?

(b) Assume a hard-switching mode with $\Delta = -0.1$ V. Evaluate the voltage conversion gain of the mixer when you vary the amplitude of the LO signal, $V_{LO,ac}(t)$, from 0.2V to 2V (you can pick several points in between.).

(c) Repeat the question in (b) with $\Delta = 0.1$ V.

(Remark) In this problem we did not take into account the effect of the IF capacitance (capacitance between the two differential IF ports) which arises from the next stage input capacitance (and some parasitic cap). If you are interested, re-tackling and understanding the problem with the capacitance will be rewarding. The combination of “time-varyingness” in the mixer and the memory effect (capacitance effect) leads to interesting dynamics.

(Problem 2*) Type-I PLL Design (120pt)

Design a 1-GHz type-I PLL utilizing the devices from the *tsmc18rf* library. Use 1.8 V for V_{dd} . Do not use generic components except for inductors (You do not have to use inductors at all) and the reference frequency. For inductors, L should be smaller than 5 nH, and Q should be smaller than 10. For the reference frequency, you may use an ideal sinusoidal component around 1 GHz. For the VCO, loop filter, and phase detector, you may use any circuit topology you like. You should present

- frequency tuning curve (f vs. V_{cont}) in your VCO and approximate K_{VCO} (VCO gain);
- $\overline{V_{PD}(t)}$ vs. phase error at the input of the phase detector, and approximate K_{PD} ;
- tracking transient for reference frequency changes of a varying degree, and estimate of the track range.

This problem is not to obtain the optimal performance, but to get familiar with the basic PLL behavior and its simulation.

(Problem 3) Phase noise of a PLL-based frequency synthesizer (40pt)

In class we studied phase noise of PLLs. In this problem, we calculate phase noise of PLL-based frequency synthesizers, which contain frequency dividers between VCOs and phase detectors in PLLs: see Fig. 2. This problem is to show the impact of frequency division on phase noise of PLLs.

In Fig. 2, $F(s)$ is the overall transfer function of a phase detector followed by a simple 1-pole low-pass loop filter with the 3dB bandwidth of ω_{3dB} . $O(s)$ is the transfer function of the VCO, which is modeled as a perfect integrator as usual. Use $F(s) = (1 + s)^{-1}$ and $O(s) = s^{-1}$ assuming proper normalizations in which $K_{PD} = 1$, $K_{VCO} = 1$, and $\omega_{3dB} = 1$. In Fig. 2, $\Phi_{VCO}(s)$, $\Phi_{IN}(s)$, and $\Phi_{FS}(s)$ correspond to phase noise of the VCO, phase noise of the input reference signal, and phase noise of the frequency synthesizer, respectively: $\Phi_{VCO}(s)$ and $\Phi_{IN}(s)$ are the causes of $\Phi_{FS}(s)$.

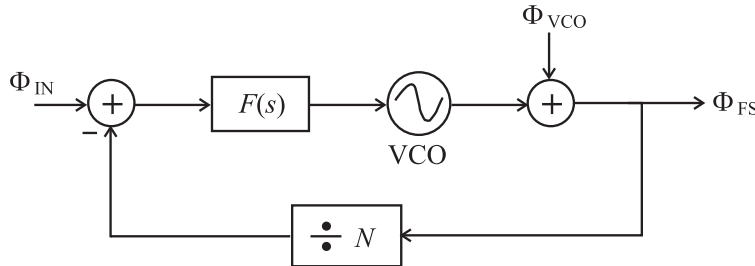


Figure 2: Phase noise of a frequency synthesizer.

(a) Assume that $\Phi_{IN}(s) = 0$ and the VCO is the only noise source. Assume that the VCO phase noise, $\Phi_{VCO}(s)$, has the power spectral density of

$$S_{\phi,VCO}(\omega) = \frac{1}{\omega^2} \quad (5)$$

supposing that only white noise sources exist in the VCO. You should be familiar with this expression from Homework #5. The proportional constant was set to 1 for brevity. Calculate the power spectral density of the frequency synthesizer phase noise $\Phi_{FS}(s)$, that is, $S_{\phi,FS}(\omega)$, for $N = 1$ (no frequency divider) and for $N = 10$. Plot the Bode plots for $S_{\phi,VCO}(\omega)$, $S_{\phi,FS}(\omega; N = 1)$, and $S_{\phi,FS}(\omega; N = 10)$. How does the frequency division affect the frequency synthesizer phase noise? Sketch $S_{v,FS}(\omega)$ (power spectral density of the voltage signal of the frequency synthesizer) *qualitatively* for $N = 1$ and $N = 10$.

(b) Now assume a noiseless VCO and that the input reference frequency signal is the only noise source, whose phase noise, $\Phi_{IN}(s)$, has the power spectral density of

$$S_{\phi,IN}(\omega) = \frac{1}{\omega^2} \quad (6)$$

Calculate the power spectral density $S_{\phi,FS}(\omega)$ of the frequency synthesizer phase noise for $N = 1$ and $N = 10$. Plot the Bode plots for $S_{\phi,IN}(\omega)$, $S_{\phi,FS}(\omega; N = 1)$, and $S_{\phi,FS}(\omega; N = 10)$. How does the frequency division affect the frequency synthesizer phase noise? Sketch $S_{v,FS}(\omega)$ for $N = 1$ and $N = 10$.

(*Remark*) Similarly you can calculate the frequency synthesizer phase noise originating from the frequency divider noise.

(*Suggested reading*) A. J. Viterbi, "Phase-locked loop dynamics in the presence of noise by Fokker-Planck techniques," *Proceedings of IEEE*, pp. 1737-1753, 1963.