

# ES 272 Final Project - Spring, 2009

## “Design of an Integer- $N$ Frequency Synthesizer”

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 Due: May 22nd, 2009  
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The goal of this final project is to design an integer- $N$  PLL-based frequency synthesizer. Figure 1(a) shows an overall architecture of the integer- $N$  PLL frequency synthesizer to be designed. The target design specifications are summarized in Table 1. The reference clock has a frequency of 528 MHz, and hence the channel spacing is the same frequency of 528 MHz. The frequency divider should be capable of four division ratios of 12, 13, 14, and 15, to produce output frequencies of 6.336 GHz, 6.864 GHz, 7.392 GHz, and 7.920 GHz. Throughout this project, use the ideal sinusoidal differential VCO saved as **VCO\_VA** in the *ES272lib* library. The key character of this VCO is shown in Fig. 1(b). For the reference clock, use a 528-MHz pulse generator, followed by two inverters as shown in Fig. 1(c).

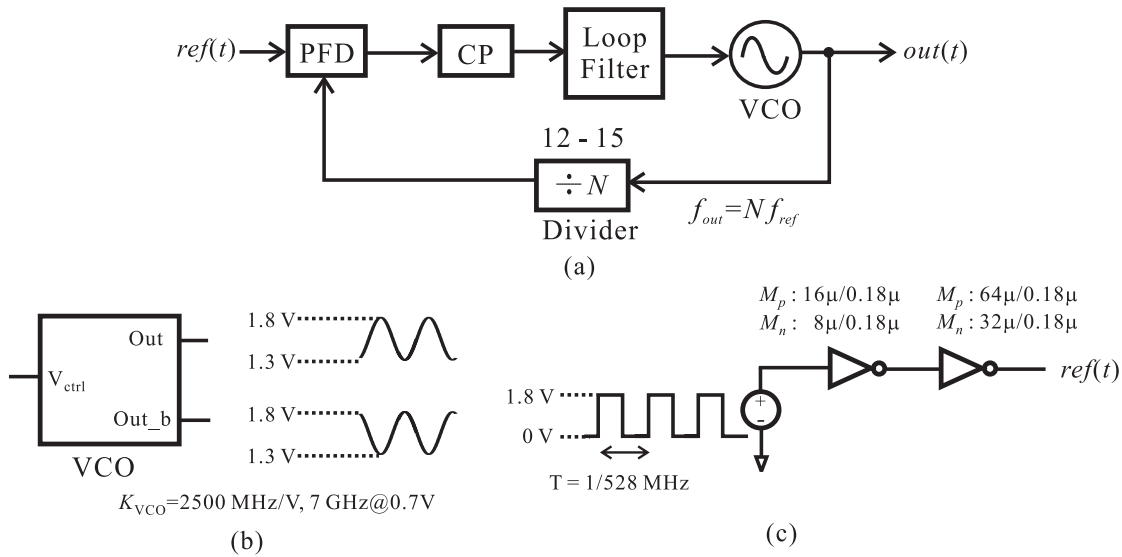


Figure 1: (a) Overall architecture of the integer- $N$  frequency synthesizer. (b) Key character of the VCO to be used. The VCO is saved as **VCO\_VA** in the *ES272lib* library. (c) Reference clock generation scheme.

Table 1: Design Specification

Technology	0.18 $\mu\text{m}$ CMOS
Voltage Supply	1.8 V
Reference frequency (Channel spacing)	528 MHz
Output frequency	6.336 GHz, 6.864 GHz, 7.392 GHz, and 7.920 GHz
Maximum current in the freq. divider	20 mA
Maximum current in the rest blocks	5 mA
Settling time (for a 528 MHz step)	< 300 ns

## Part-I: Frequency Divider Design (300 points)

The first part of this project is to design the frequency divider, which is usually one of the most challenging tasks in the overall frequency synthesizer design. The frequency divider should meet the following specifications.

- Division ratios: 12, 13, 14, and 15.
- Input frequency range: 6-to-8 GHz. Use the VCO of Fig. 1(b) for the input.
- Output level: The full CMOS level, that is, the full swing from 0 to 1.8 V while driving a 20 fF capacitor load.
- Maximum current consumption allowed: 20 mA (no limit on biasing circuits)

Figure 2 shows a scheme to test the frequency divider.

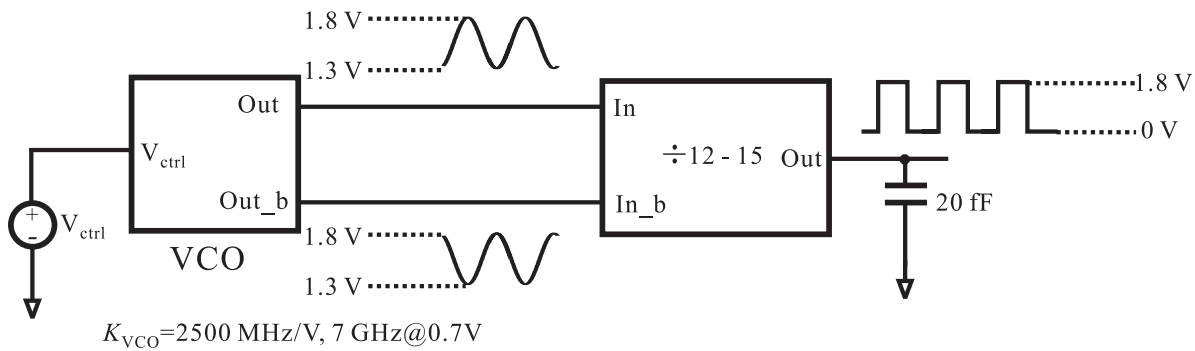


Figure 2: Frequency divider test scheme.

You may use any architecture you'd like to use for the frequency divider. An example frequency divider architecture is depicted in Fig. 3. Figures 4 - 7 show how the building blocks of the frequency divider of Fig. 3 may be realized. You are allowed to use ideal resistors from the *Analog Libraries*. Inductors are not allowed in this project (the reason for this statement is because a shunt-peaking using inductors could boost the speed of the frequency divider). Use ideal current and voltage sources for biasing and power supply.

### Report #1

Your report should include contents described below, and must be no longer than 15 pages including plots of simulated data. This 15-page limit excludes schematic drawings.

- Summary of your design procedure.
- Summary of the divider performance for the followings:
  1. Maximum input frequency of the overall frequency divider (the frequency range requirement is to go up to 8 GHz, but try to see how farther it can go beyond 8 GHz).
  2. Maximum input frequency for each major block of the frequency divider. For example, in the case of the frequency divider of Fig. 3, report the maximum input frequency for the dual-modulus 4/5 prescaler, the static divide-by-3, and the CML-to-CMOS converter.

3. Total power dissipation at an input frequency of 8 GHz (excluding bias circuits).
4. A break-down of power dissipations among major blocks in the divider at an input frequency of 8 GHz.

- Summary of your simulated results, including the divider input waveforms and the output waveforms of each major building block of your frequency divider, at several different frequencies in the target frequency range of 6-to-8 GHz. The plots must clearly show that you can switch among the division values (12, 13, 14, and 15) to attain proper output frequencies in the same transient simulation run.

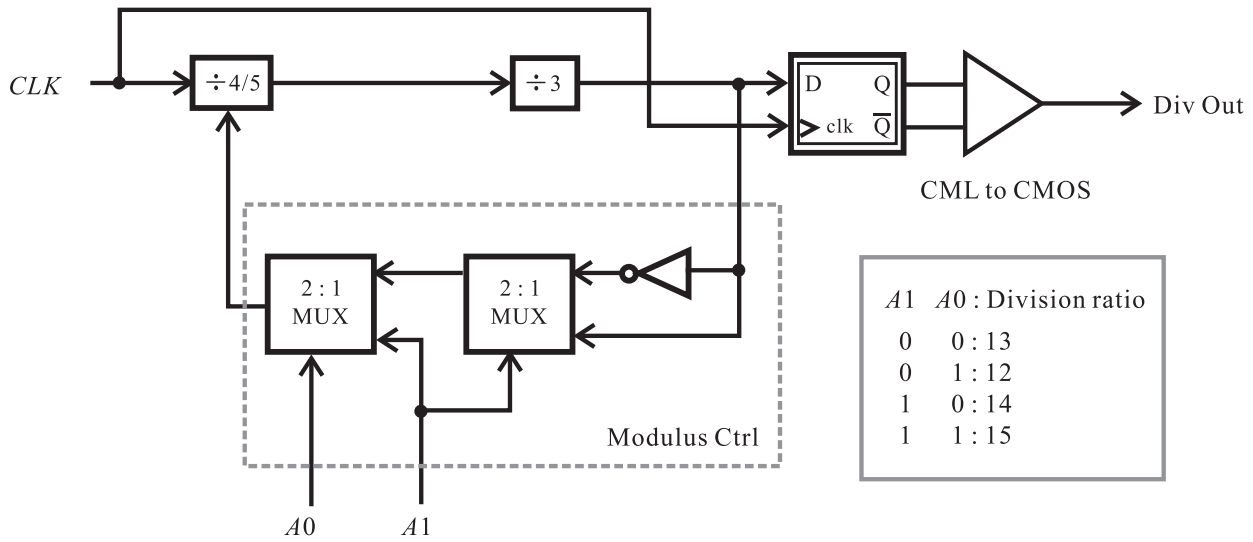


Figure 3: An example frequency divider. Implementation examples for major building blocks of this frequency divider are shown in Figs. 4 - 7.

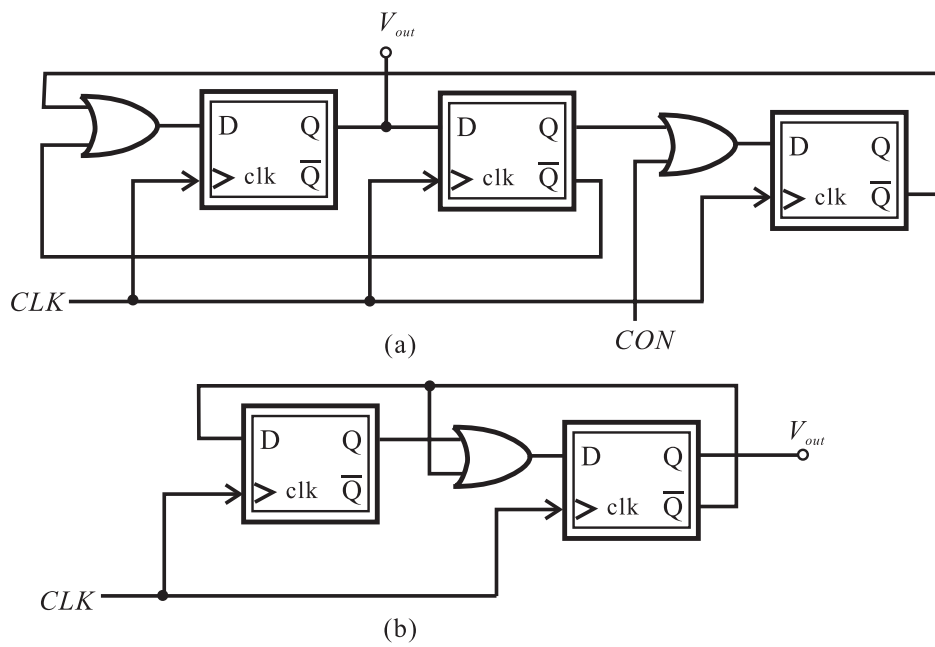


Figure 4: (a) Example implementation of the dual-modulus 4/5 prescaler of Fig. 3. (b) Example implementation of the static divide-by-3 of Fig. 3.

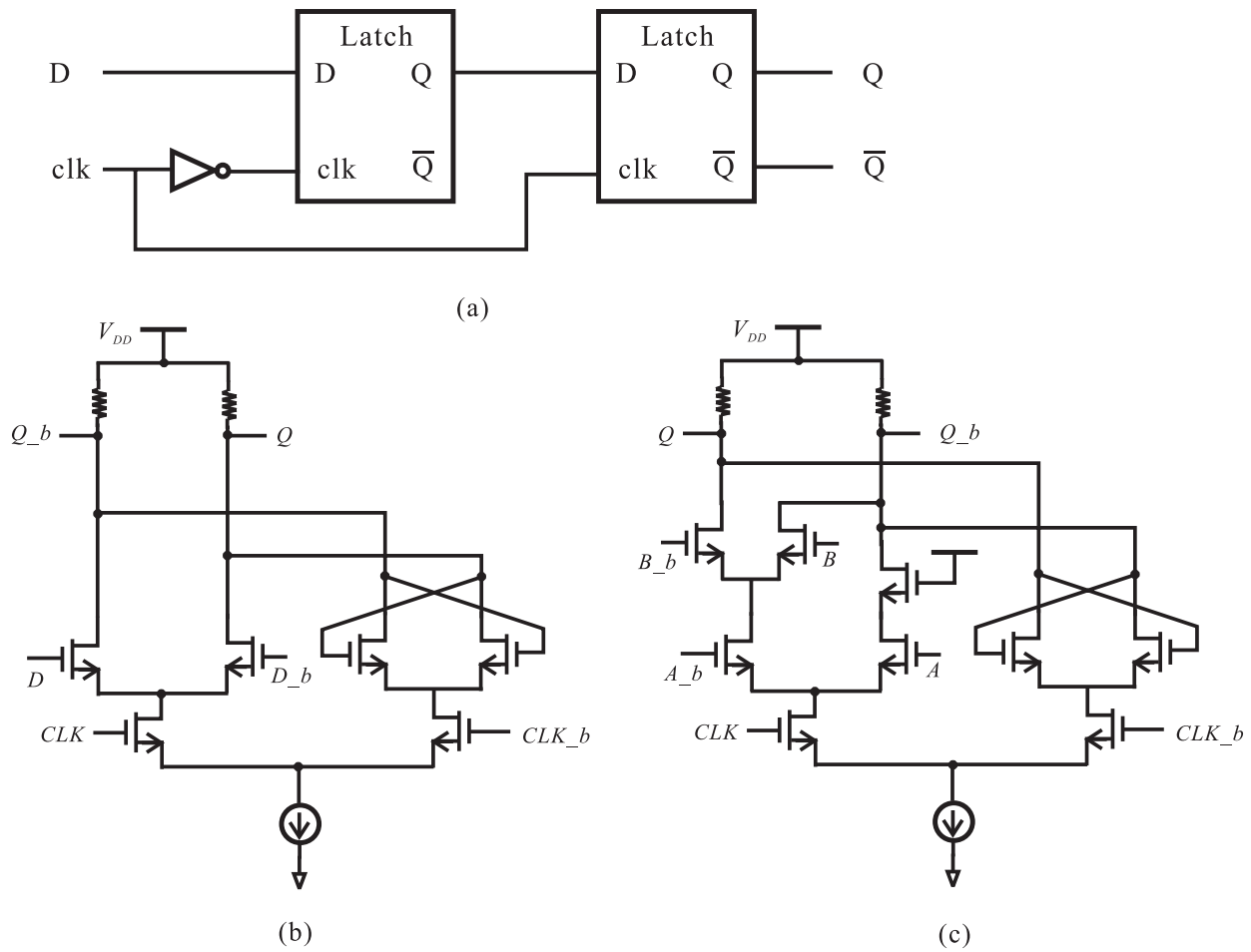


Figure 5: (a) The D-flip-flops of Figs. 3 and 4 may be implemented as shown here. (b) The latch circuits of Fig. 5(a) may be implemented as shown here using the current mode logic (CML) [Page 3 of Lecture Note # 18]. The CML is preferred, and often necessary, due to the high-speed operation. (c) Example of a CML latch with an OR gate.

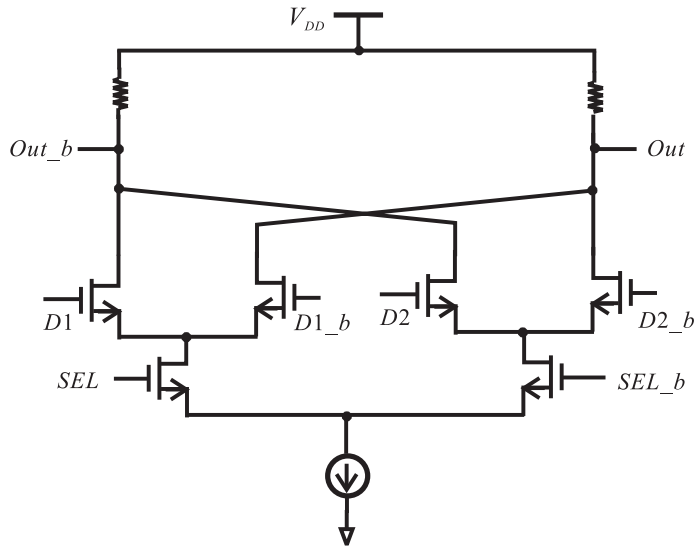


Figure 6: Example implementation of the multiplexers of Fig. 3.

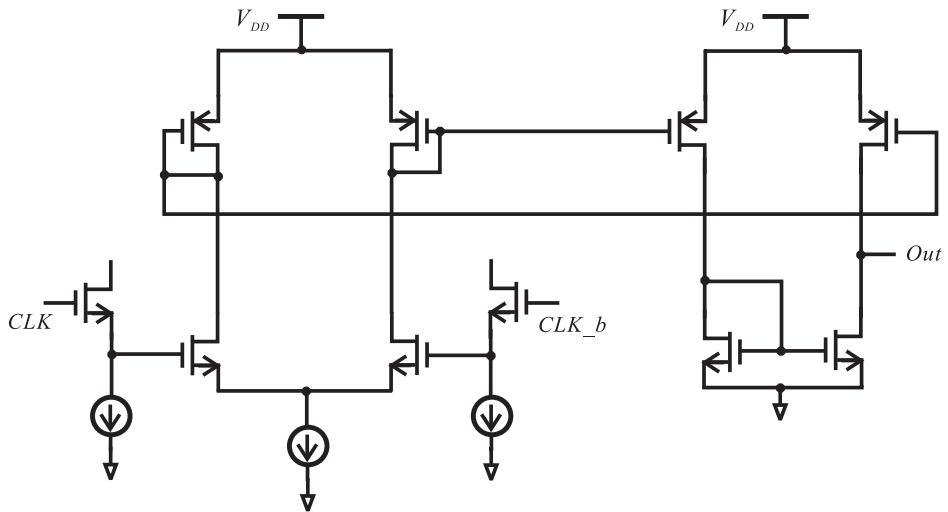


Figure 7: Example implementation of the CML-to-CMOS converter of Fig. 3.

## Part-II: Integer- $N$ Frequency Synthesizer Design (300 points)

The second part of this project is to design the overall integer- $N$  frequency synthesizer of Fig. 1, using the frequency divider you designed in Part-I while designing the remaining blocks such as the charge-pump and PFD. You must use a passive 2nd- or 3rd-order loop filter. You may use ideal resistor and capacitor from the *Analog Libraries* for your loop filter. Following is the summary of the design specifications for the integer- $N$  frequency synthesizer (repetition of Table 1).

- Reference frequency (channel spacing) : 528 MHz
- Output frequencies : 6.336 GHz, 6.864 GHz, 7.392 GHz, and 7.920 GHz
- Maximum current (excluding biasing circuits and the frequency divider) : 5 mA
- Settling time (for a 528 MHz step) < 300 ns

You are free to choose any architecture for the charge-pump and PFD. The following paper may be useful in understanding advanced charge-pump design issues.

W. Rhee, "Design of high-performance CMOS charge pumps in phase-locked loops," *Proceedings of the 1999 ISCAS*, vol. 2, pp. 545-548, May. 1999.

The following papers may be useful for the advanced PFD design.

M. Mansuri, D. Liu, and C. Yang, "Fast frequency acquisition phase-frequency detectors for GSamples/s phase-locked loops," *IEEE J. Solid-State Circuits.*, vol. 37, no. 10, pp. 1331-1334, Oct. 2002.

H. Johansson, "A simple precharged CMOS phase frequency detector," *IEEE J. Solid-State Circuits.*, vol.33, no. 2, pp. 295-299, Feb. 1998.

K. Lee, B. Park, H. Lee, and M. Yoh, "Phase frequency detectors for fast frequency acquisition in zero-dead-zone CPPLLs for mobile communication systems," *Proc. ESSCIRC.*, p. 525, Sep. 2003.

### **Report #2**

Your report should include contents described below, and must be no longer than 15 pages including plots of simulated data. This 15-page limit excludes schematic drawings.

- Summary of your design procedure. It must include Bode plots for the loop bandwidth design.
- Summary of the frequency synthesizer performance for the followings:
  1. Synthesized output frequencies.
  2. Settling times for the following frequency division ratio changes:  $12 \rightarrow 13$ ,  $13 \rightarrow 14$ ,  $14 \rightarrow 15$ ,  $15 \rightarrow 14$ ,  $14 \rightarrow 13$ ,  $13 \rightarrow 12$ )
  3. Total power dissipation at each of the 4 desired output frequencies (excluding bias circuits).
  4. A break-down of power dissipation among major building blocks of the frequency synthesizer.
  5. The size of control voltage ripples at each of the 4 desired output frequencies.