ES 272 Assignment #3
Due: April 29th, 2014; 10am sharp, in the dropbox outside MD 131 (Donhee Ham office)
Instructor: Donhee Ham (copyright ©2014 by D. Ham)

(Problem 1) Noise figure (70pt)

Consider an NMR experiment (which we talked about in depth in class). The spin precession motions induce an RF voltage signal across a solenoidal coil that surrounds the sample under test. Since this RF signal is very weak, a low-noise amplifier (LNA)—voltage amplifier—is used to enhance the signal. This problem considers how to interface the coil with the LNA in order to minimize the LNA’s noise figure. The intention of this problem is to highlight the concept of the noise figure, for which the NMR experiment offers a nice context.

The coil and induced RF voltage signal may be modeled as in Fig. 1(a), which includes: coil inductance $L$; the induced RF voltage signal, whose $rms$ value is $V_{rms}$; parasitic coil resistance $R$; thermal noise, $v^2_n/\Delta f = 4kTR$, generated by $R$. For numerical calculations in certain parts of this problem, use $L = 500$ nH, $R = 4.2$ Ω, and $f_0 = \omega_0/(2\pi) = 21$ MHz (spin precession frequency). The quality factor of the inductor is $Q = \omega_0 L/R \approx 16$. Assume that the signal bandwidth is 1.1 kHz (this non-zero signal bandwidth arises due, for instance, to the magnetic field inhomogeneity).

For the LNA shown in Fig. 1(b), assume that it has been already designed and has the following fixed properties: infinite input impedance, $Z_{LNA} = \infty$; input-referred voltage noise of $(v^2_i/\Delta f)^{1/2} = 1.3$ nV/√Hz; zero input-referred current noise (this zero current noise is a consequence of $Z_{LNA} = \infty$). Do you understand this statement?

(a) We begin by directly connecting the LNA and the coil as in Fig. 1(c). Show that the LNA’s noise figure is given by

$$NF = 10 \cdot \log\left[\frac{v^2_n + v^2_i}{v^2_n}\right]$$

(1)

where $v^2_n$ is the coil noise over the entire signal bandwidth (1.1 kHz), i.e., $v^2_n = v^2_n/\Delta f \times 1.1$ kHz, and $v^2_i$ is the LNA’s input-referred voltage noise over the entire signal bandwidth, i.e., $v^2_i = v^2_i/\Delta f \times 1.1$ kHz. Calculate the numerical value for the noise figure in dB. The noise figure should be very high. Can you explain why, without resorting to (1), but by arguing how the signal-to-noise ratio gets deteriorated through the LNA?

(b) To reduce the noise figure, we can insert a passive network between the coil and the LNA as shown in Fig. 1(d). The passive network won’t amplify its input power, but it can amplify its input voltage: both the signal $V_{rms}$ and noise $v^2_n$ of the coil are re-scaled, or, passively amplified, by the network by a certain gain factor, $\alpha > 0$, whose value depends on a specific arrangement of the passive network ($\alpha$ is the magnitude of the transfer function of the passive network at the design frequency). By considering how the signal-to-noise ratio changes through the circuit, argue that the noise figure will be minimized when $\alpha$ is maximized. Quantitatively, show that the noise figure of the LNA is given by

$$NF = 10 \cdot \log\left[\frac{\alpha^2 v^2_n + v^2_i}{\alpha^2 v^2_n}\right]$$

(2)

This equation confirms that a maximum $\alpha$ corresponds to a minimum noise figure.

(c) Now we go further and design an optimum passive network that yields a maximum $\alpha$. Various topologies may be considered, and here, we try the $C_1-C_2$ network shown in Fig. 1(e). Analytically express $C_1$ and $C_2$ that maximize $\alpha$, in terms of given parameters. The expressions will be simplified if you use $Q$ of the inductor as one parameter. Analytically express the corresponding maximum $\alpha$. What physical situation does your optimum solution correspond to? What is the corresponding minimum noise figure, numerically

1
(in dB), and how does it compare to part (a)? In this optimal case, what is the input impedance $Z_c$ (analytically) shown in Fig. 1(e)? Is $Z_c$ matched to $Z_{LNA}$?

(d) Now imagine a situation where we cannot avoid using a transmission line (with fixed length $l$, characteristic impedance $Z_0$, wave propagation velocity of $v$, and propagation constant $\beta$) in connecting the LNA and the coil, as shown in Fig. 1(f). This is an often-met scenario in traditional NMR experiment, where the coil and the LNA cannot be placed in physical proximity. In such a case, the optimum passive network that minimizes the noise figure should include the transmission line. We also include a capacitor $C_1$ in the passive network, which is deliberately added in parallel to the coil [Fig. 1(f)]. Analytically express the optimum value of $C_1$ that maximizes $\alpha$, in terms of the given parameters, and also, analytically express the corresponding maximum $\alpha$. Assume that $\beta l \ll 1$ and use first-order approximation in your calculation, and assume negligible loss in the line. What is the minimum noise figure (numerically, in dB) corresponding to the maximum $\alpha$?
Figure 1: Noise figure.
(Problem 2) Inductive-peaking (60pt)

Figure 2 shows a MOSFET amplifier. The transistor is biased in the pinch-off region with a transconductance of $g_m$. The transistor size and the values of $R$ and $C$ are fixed, while the inductance, $L$, is a design parameter (Neglect all the transistor parasitics). The gain characteristic or frequency response of the amplifier can be controlled by altering the value of $L$. In this problem, we seek to obtain the maximum-bandwidth and maximally-flat frequency responses.

(a) Show that the amplifier’s small-signal voltage gain (frequency response) normalized to its dc gain, $g_m R$, is given by

$$H(x) \equiv \frac{|A_v|}{g_m R} = \sqrt{\frac{1 + (\alpha x)^2}{(1 - \alpha x^2)^2 + x^2}}$$

where $\omega_{3dB,0} \equiv (RC)^{-1}$ is the 3dB bandwidth of the uncompensated ($L = 0$) amplifier, $x \equiv \omega / \omega_{3dB,0}$ is the normalized frequency, and $\alpha \equiv L \cdot (\omega_{3dB,0}/R)$ proportional to $L$ is the design parameter. Plot $H(x)$ versus $x$ for $\alpha = 0, 0.2, 0.4, 0.6, \text{and} 0.8$.

(b) Express the 3dB bandwidth, $\omega_{3dB}$, of the amplifier in terms of $\omega_{3dB,0}$ and $\alpha$. Find $\alpha$ at which $\omega_{3dB}$ becomes maximum. Calculate the ratio of this maximum bandwidth to $\omega_{3dB,0}$. Estimate the peaking in the frequency response (maximum of $H(x)$) in this maximum-bandwidth design.

(c) If $dH(x)/dx \leq 0$ for all $x \geq 0$, the frequency response is called flat. Find the maximum $\alpha$ with which $H(x)$ is flat. This $\alpha$ corresponds to the so-called “maximally-flat” response (do you understand why?). What is $\omega_{3dB}$ in this maximally-flat design?

(Problem 3) Amplifier nonlinearity (30pt)

(a) An amplifier with 20 dB of power gain has a third-order intercept of 30 dBm at the output. If the input consists of a 0 dBm signal at 1 GHz and another 0 dBm signal at 1.05 GHz, what will be the output power of the third-order products at 1.1 GHz and 0.95 GHz?

(b) The same as Problem 1(a) except that input signal at 1 GHz increases in power to 10 dBm while the input signal at 1.05 GHz remains at 0 dBm.
(Problem 4) Distributed amplifier (80pt)

Here we revisit the distributed amplifier discussed in class to fill in some details omitted in class. We will also consider a case more general than what we discussed in class.

(a) Consider a distributed amplifier with $N$ distributed MOS transistors: Fig. 3. The input and output artificial transmission lines are identical (the same $C$ and $L$), thus, the wave velocity in the input line is the same as that in the output line. Parasitic capacitors of MOS transistors are absorbed into the artificial lines, contributing to the line capacitors (gate-drain parasitic capacitors are ignored). Each transistor has a transconductance of $g_m$ (bias is not shown in the figure). The input and output lines are terminated with the image impedances.

Let the small-signal gate and drain voltages of the $k$-th ($k=1, 2, 3, ..., N$) MOS transistor be $a_k$ and $b_k$, respectively. Assume that they are sinusoidal waves with angular frequency $\omega$. Derive the following recursive relations for $k=1, 2, 3, ..., N-1$:

\begin{align*}
a_{k+1} &= a_k e^{-j\beta} \\
b_1 &= -a_1 g_m Z_{\text{middle}} \\
b_{k+1} &= b_k e^{-j\beta} - a_{k+1} g_m Z_{\text{middle}}
\end{align*}

where $Z_{\text{middle}}$ is as discussed in class and $\beta = \cos^{-1}[1 - 2(\omega/\omega_c)^2]$. Using these recursive relations, show that the voltage gain $A_v = b_N/a_1$ and its magnitude are given by

\begin{align*}
A_v &= -Ng_m Z_{\text{middle}} \cdot e^{-j(N-1)\phi} \\
|A_v(\omega)| &= \frac{Ng_m Z_0}{2} \cdot \frac{1}{\sqrt{1 - \omega^2/\omega_c^2}}
\end{align*}

In class, we studied the implication of (8): as we increase the number of transistors and reduce each transistor size proportionally, or as the circuit is more distributed, the degree of “lumpedness” of the circuit is
reduced, and the cutoff frequency of the artificial lines is increased while maintaining the same gain, hence enhancing the gain-bandwidth product indefinitely.

(b) The amplifier gain $A_v(\omega)$ in (8) diverges to infinity at the cutoff frequency. This problem, however, can be circumvented, or more specifically, $A_v(\omega)$ can be made attenuate near cutoff frequencies, by deliberately mismatching the phase delay of the input line and that of the output line. To see this, let the lumped inductors and capacitors in the input line be $L_g$ and $C_g$, and those in the output line be $L_d$ and $C_d$. The phase delay, cutoff frequency, image impedance, etc., of the input line are now different from those of the output line. Derive $A_v(\omega)$. Plot $|A_v(\omega)|$ versus $\omega$ for various phase delay mismatches. Can you make $A_v(\omega)$ maximally flat by properly adjusting the phase delay mismatch (you don’t have to be analytically rigorous)?

(Problem 5) Diode Ring Mixer (50pt)

The diode ring circuit of Fig. 4 is a mixer. In this problem we analyze the diode ring mixer assuming that the RF signal, $V_1(t) = a \cos(\omega_{RF}t + \phi)$, is very small as compared to the local oscillator signal, $V_2(t) = b \cos(\omega_{LO}t)$, that is, $a \ll b$ ($a > 0$ and $b > 0$).

![Figure 4: Diode ring mixer](image)

Since $a \ll b$, when the oscillator output ($V_2$) is positive, diodes D2 and D3 conduct while the other two diodes are off. The situation turns the other way around when the oscillator output reverses its polarity. Overall diodes D2 and D3 conduct for positive half cycles of the oscillator while diodes D1 and D4 conduct for negative half cycles. Assuming that the diode resistance under the forward-biased condition is $r_d$ and both of the transformers have 1:1 turn ratio, show that

$$V_{IF}(t) = V_1(t) \cdot \frac{R}{2R + r_d}$$

for a positive half cycle of $V_2$, and

$$V_{IF}(t) = -V_1(t) \cdot \frac{R}{2R + r_d}$$

(9)

(10)
for a negative half-cycle of $V_2$. Based on (9) and (10), explain how frequency down conversion is achieved in the diode ring mixer, and calculate the mixer’s voltage conversion gain (ratio of the IF voltage amplitude to the RF voltage amplitude).

(Problem 6) MOS Switching Mixer (70pt)

Figures 5(a) shows a differential CMOS passive switching mixer. Transistors $M_1$ and $M_4$ are driven by a sinusoidal local oscillator (LO) with a frequency of $f_{LO}$ while transistors $M_2$ and $M_3$ are driven by the opposite phase of the same LO. Since the LO signal amplitude is typically substantially larger than the RF and IF signal amplitudes and the RF and IF signals have more or less the same $dc$ values due to the circuit configuration, all of the MOS transistors operate between “off” and “on (triode)” regimes.

How the passive mixer multiplies the RF and LO signals to give the IF signal can be understood in the following way. When transistors $M_1$ and $M_4$ are on while $M_2$ and $M_3$ are off, $V_{IF} = V_{+IF} - V_{-IF} \approx V_{+RF} - V_{-RF} \equiv V_{RF}$. Likewise when transistors $M_2$ and $M_3$ are on while $M_1$ and $M_4$ are off, $V_{IF} \approx -V_{RF}$.

Therefore, $V_{IF}(t)$ is essentially $V_{RF}(t)$ multiplied by a periodic square pulse signal alternating between 1 and $-1$ with a period of $1/f_{LO}$.

![Figure 5: CMOS quad switching mixer](image)

The above explanation, while capturing the essence, assumed that the $M_1$ - $M_4$ pair turns on immediately after $M_2$ - $M_3$ pair turns off and vice versa. This represents only one among three possible switching modes, which will be explained shortly. In this problem, you are asked to calculate the voltage conversion gain ($\equiv |V_{IF}|/|V_{RF}|$) of the passive switching mixer in the various switching modes.

Figure 5(b) shows the equivalent switch model for the CMOS passive mixer. In the equivalent model, $g(t)$ represents the time-dependent (modulated by LO and RF signals) channel conductance of the MOS transistors, and when the transistor is in the triode-off regime, $g(t)$ is given by

$$g(t) = \mu_n C_{ox} \frac{W}{L} [V_{gs}(t) - V_{ds}(t) - V_{th}]$$

(11)

where $\mu_n$, $C_{ox}$, $L$, and $W$ are defined as usual, while $V_{gs}(t)$ is the gate-source voltage, $V_{ds}(t)$ is the drain-source voltage, and $V_{th}$ is the threshold voltage of the MOS transistors. While $V_{th}$ is time-dependent in
general due to the body effect of the MOS transistors, here, it is regarded as constant to avoid complication. Since the LO signal amplitude is significantly larger than the RF signal amplitude, we can approximate the triod-regime channel conductance, $g(t)$, in the above as

$$g(t) \approx \mu_n C_{ox} \frac{W}{L} [V_{LO,ac}(t) + V_{LO,dc} - V_{RF,dc} - V_{th}]$$

(12)

Incorporating the transistors’ off period, $g(t)$ can be more generally expressed as

$$g(t) \approx \begin{cases} \mu_n C_{ox} \frac{W}{L} [V_{LO,ac}(t) + V_{LO,dc} - V_{RF,dc} - V_{th}] & \text{(on & triode: } g(t) > 0) \\ 0 & \text{(off)} \end{cases}$$

(13)

which is periodic in $f_{LO}$. In Fig. 5(b), $\overline{g}(t)$ is simply the 180° phase-shifted-version of $g(t)$.

From Fig. 5 and Eq. (13), we can see that the three switching modes briefly mentioned earlier are: hard-switching, perfect-switching, and soft-switching, where the criterion to determine the switching mode is given by

$$\Delta \equiv V_{LO,dc} - V_{RF,dc} - V_{th}$$

1. $< 0$ (hard-switching)
2. $= 0$ (perfect-switching)
3. $> 0$ (soft-switching)

(14)

In the hard-switching mode, there is a period of time during which all transistors are off. In the soft-switching mode, there is a period of time during which all transistors are on. The perfect switching mode is at the borderline between the hard- and soft-switching modes, that is, $M_1 - M_4$ pair turns on immediately after $M_2 - M_3$ pair turns off and vice versa (this is the switching mode used in the second paragraph of this problem). By altering the $dc$ biases of the LO and RF signals, one can go from one switching mode to another.

(a) Calculate the voltage conversion gain of the mixer in the perfect-switching mode ($\Delta = 0$). Is the voltage conversion gain a function of the LO signal amplitude in the perfect-switching mode?

(b) Assume a hard-switching mode with $\Delta = -0.1$ V. Evaluate the voltage conversion gain of the mixer when you vary the amplitude of the LO signal, $V_{LO,ac}(t)$, from 0.2V to 2V (you can pick several points in between.).

(c) Repeat the question in (b) with $\Delta = 0.1$ V.

(Remark) In this problem we did not take into account the effect of the IF capacitance (capacitance between the two differential IF ports) which arises from the next stage input capacitance (and some parasitic cap). If you are interested, re-tackling and understanding the problem with the capacitance will be rewarding. The combination of “time-varyingness” in the mixer and the memory effect (capacitance effect) leads to reasonably interesting dynamics.