Other flip-flops, such as the D-type clocked flip-flop, have more internal complexity but are easier to program.

- Digital blocks are usually found in IC form, ranging from small-scale integration (SSI, 2 to 4 blocks per IC) to very-large-scale integration (VLSI, 250,000 or more blocks per IC). Large, powerful ICs cost very little more than small ICs.
- Digital blocks made with one particular fabrication technology are said to belong to a particular *logic family*. Several different logic families exist and are used for different purposes. In general, blocks of one family are compatible with other blocks of that family but not with those of other families.

PROBLEMS

Section 11.1

11.1 A time-varying voltage represents a series of binary numbers. Let the "high" range be 4 to 5 V and the "low" range 0 to 0.8 V. Assume that positive logic is used. Sketch a possible waveform representing the binary digits 10011010.

11.2 Explain the following:
- **a.** The binary digit 1.
- **b.** A switching variable.
- **c.** The logical state **1**.
- **d.** The "high" range.

Section 11.2

11.3 Obtain the truth tables for the blocks shown in Fig. 11.30(a), (b), and (c).

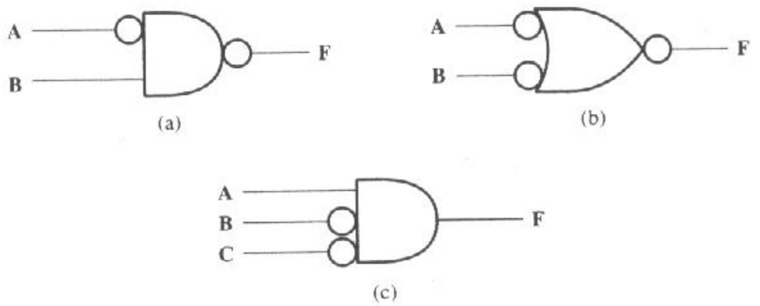
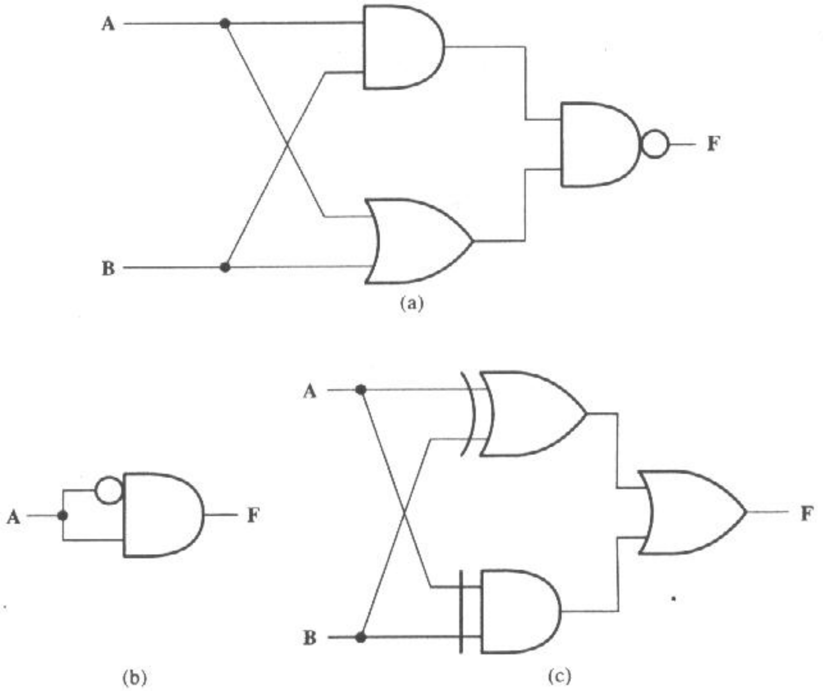


FIGURE 11.30

✓**11.4** Obtain the truth table for the connections shown in Fig. 11.31(a), (b), and (c). For parts (b) and (c) explain why the answers come out as they do.



(a)

(b)

(c)

FIGURE 11.31

11.5 Write logical (Boolean algebra) expressions for the blocks shown in Fig. 11.30.

11.6 Write logical (Boolean algebra) expressions for the connections shown in Fig. 11.31.

11.7 Let the electrical output of a block be related to the electrical inputs as shown in Fig. 11.32. What logical block or combination of blocks describes this electrical operation if the negative-logic convention is adopted? If the positive-logic convention is adopted?

Input A	Input B	Output F
low	low	high
low	high	low
high	low	low
high	high	high

FIGURE 11.32

11.8 Find the values (**0** or **1**) of the following:

a. **(1 + 0) 1**

b. $0 + (1\overline{1})\,1$

c. $(\overline{1 + 0})\,(1 + 1)$

11.9 Write the truth tables for the following switching functions:

a. $\mathbf{F} = (\mathbf{X} + \mathbf{Y})\,\overline{\mathbf{X}}$

b. $\mathbf{F} = (\mathbf{Y} \cdot \mathbf{Z})\,\overline{\mathbf{X}} + \mathbf{X}$

11.10 Any truth table defines a switching function.

a. How many *different* switching functions of two input variables exist?

b. Give an example of one that is not in Table 11.1.

c. How many different switching functions of three variables exist?

11.11 Show, by constructing truth tables, the following:

a. $(\mathbf{A})(\mathbf{1}) = \mathbf{A}$

b. $\mathbf{A} + \overline{\mathbf{A}} = \mathbf{1}$

Note: **(A)(1)** means **A AND 1**.

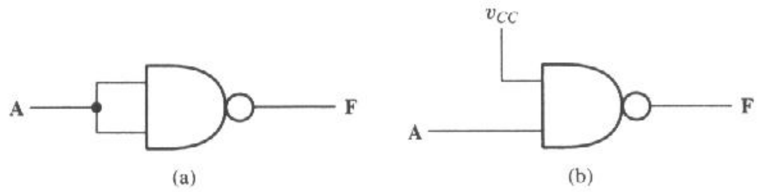
11.12 Show, by means of truth tables, that $\mathbf{A}(\mathbf{A} + \mathbf{B}) = \mathbf{A}$.

11.13 Show, by means of truth tables, that $\mathbf{A} + \mathbf{BC} = (\mathbf{A} + \mathbf{B})(\mathbf{A} + \mathbf{C})$.

11.14 Show, by means of truth tables, that $\overline{\mathbf{A}\ \mathbf{B}} = \overline{\mathbf{A}} + \overline{\mathbf{B}}$. This important result is known as *De Morgan's theorem.*

11.15 Using De Morgan's theorem (previous problem), design an **OR** gate using one **NAND** gate and two inverters.

11.16 Show that the circuits shown in Fig. 11.33(a) and (b) are each equivalent to inverters. In Fig. 11.33(b) the input marked V_{CC} is connected to the highest power-supply voltage and is therefore a permanent **1**.



(a) (b)

FIGURE 11.33

11.17 Using the results of Problems 11.14 and 11.16 and Fig. 11.12, show how to construct an **EXCLUSIVE OR** gate using only **NAND** gates. (Note that in a similar way *any* switching function can be realized using only **NAND** gates.)

11.18 Design a circuit equivalent to a two-input **COINCIDENCE** gate using two **AND** gates, one **OR** gate, and inverters.

11.19 Let *ABC* be a three-digit binary number. The number is said to have *even parity* if an even number of its digits (or none of them) is 1; otherwise it has *odd parity*. (Examples: 110 has even parity; 010 has odd parity.) Design a circuit whose output **F** is **1** if and only if the three inputs **A B C** have odd parity. (*Suggestion:* First construct the desired truth table, then realize it. Three-input gates may be used.) This circuit is called a *parity checker*.

✓ ***11.20** The voltages appearing on four wires are V_A, V_B, V_C, and V_D, corresponding to the four switching variables **A**, **B**, **C**, and **D**. Design a circuit that gives output **F** = **1** if and only if **A B C D** = **1010**. Use only **NAND** gates with two inputs each. (See Problems 11.14 to 11.16.)

✓ ***11.21** An important circuit for use in computers is a comparator, which has zero output unless the inputs are identical. Synthesize a circuit that compares $A_1\,A_2$ (a two-digit binary number) with $B_1\,B_2$ (another two-digit binary number). Use only **NAND** gates.

✓ ***11.22** Many times it is useful to have a circuit that indicates if two binary numbers are equal, or, if not, which one is greater. Design a circuit which has inputs **A** and **B** and three outputs **F**, **G**, and **H**; **F** = **1** only if **A** > **B**, **G** = **1** only if **A** = **B**, and **H** = **1** only if **A** < **B**.

***11.23** Figure 11.34 shows, in symbolic form, a device often needed in digital systems, called a *multiplexer*. The purpose is to make output **F** equal to *either* input **A** or input **B**, depending on the value of control variable **C**. When **C** = **0** we want **F** = **A**, and when **C** = **1** we want **F** = **B**. Realize this device using logic blocks.

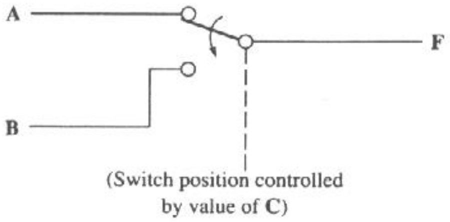
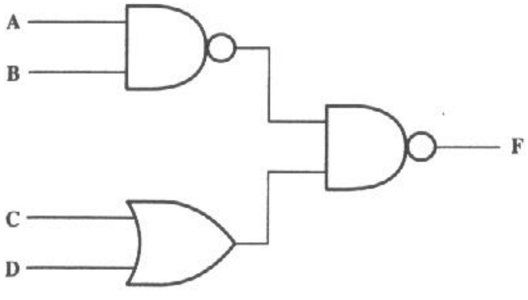


FIGURE 11.34

✓ **11.24** For the circuit shown in Fig. 11.35(a):

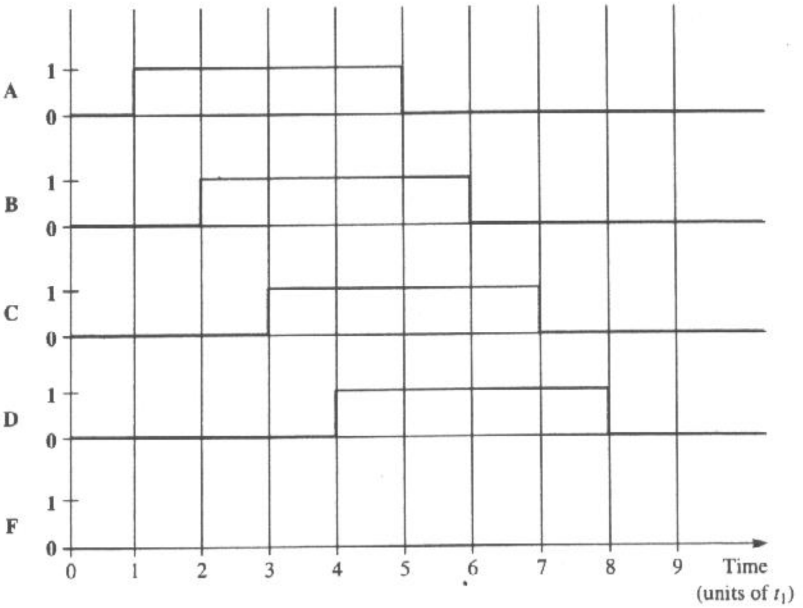
a. Construct the truth table.

b. The values of the four input variables **A B C D** as a function of time are shown in the timing diagram, Fig. 11.35(b). Fill in the variation of **F** as a function of time.



(a)

FIGURE 11.35(a)



(b)

FIGURE 11.35(b)

Section 11.3

11.25 An S-R flip-flop is used to control a camera shutter. The circuit is arranged so that when output **Q** is **1**, the shutter is opened; when **Q** = **0**, the shutter is closed. We wish to open the shutter for 1 msec exposures and to make 300 exposures per second. Make a timing diagram showing suitable **S** and **R** inputs to operate the shutter.

11.26 In Fig. 11.36, V_0 is in the "high" range and corresponds to logical **1**, while 0 V corresponds to **0**. The switch is connected to input **S** by a short wire and to input

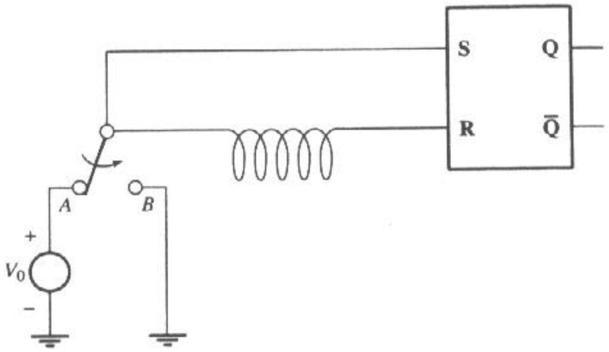


FIGURE 11.36