Solution Set 3

Exercises 12.16, 12.17, 12.18, 12.19, 12.20, 12.21, 12.22, 12.23, 12.24

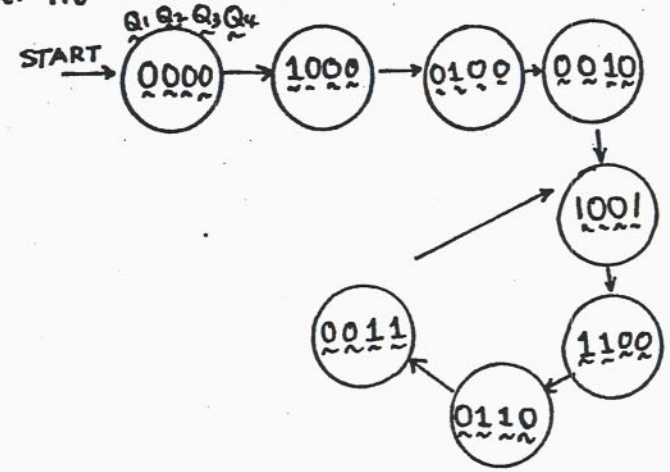
12.16

$B9_{16} = 1011\,1001$

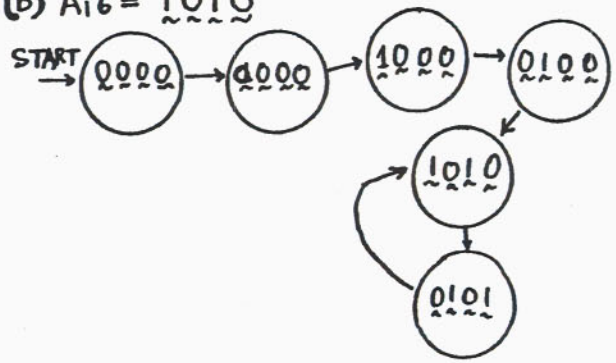
CLK	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	D_1
0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	0	0	1
3	1	0	1	0	0	0	0	0	1
4	1	1	0	1	0	0	0	0	1
5	1	1	1	0	1	0	0	0	0
6	1	1	1	1	0	1	0	0	1
7	0	1	1	1	1	0	1	0	1
8	1	0	1	1	1	1	0	1	1

12.17 LET $Q_1 Q_2 Q_3 Q_4$ BE THE OUTPUT STATE OF THE SHIFT REGISTER.

(a) $9_{16} = 1001$

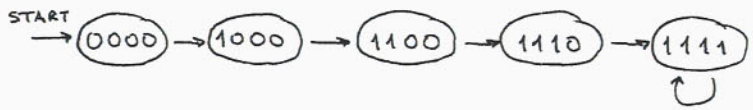


(b) $A_{16} = 1010$



(ONLY TWO STATES ARE REPEATED, SINCE 1010 HAS THE REPEATED PATTERN 10)

c) $F_{16} = 1111$



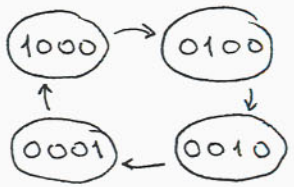
■

12.18. a)

N	I_N	Q_{1N}	Q_{2N}	Q_{3N}	Q_{4N}
0	0	1	0	0	0
1	0	0	1	0	0
2	0	0	0	1	0
3	1	0	0	0	1
4	0	1	0	0	0

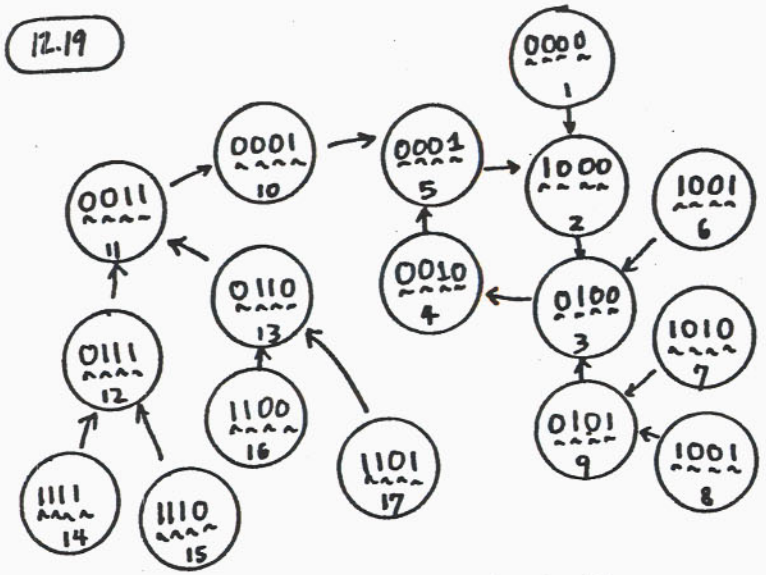
(repeats)

b)



■

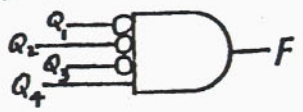
12.19



THE LIMIT CYCLE IS 2-3-4-5.

■

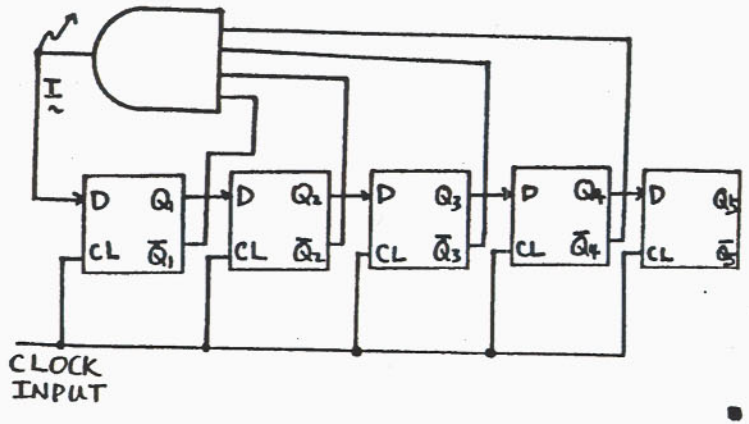
12.20 (a) ADD A DECODER TO THE OUTPUTS; FOR INSTANCE



GIVES AN OUTPUT OF 1 EACH TIME THE COUNTER RETURNS TO STATE 5.

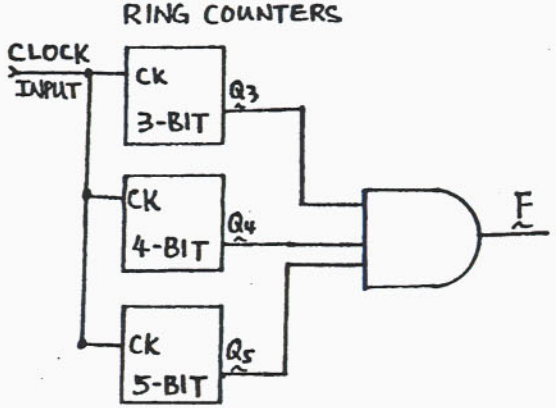
ALTERNATIVELY, ONE COULD SIMPLY USE $\underset{\sim}{I}$ AS THE OUTPUT, SINCE I GOES TO ONE EVERY TIME THE SYSTEM PASSES THROUGH STATE 5.

(b) NOW A 4-INPUT AND GATE SHOULD BE USED INSTEAD. TAKE $\underset{\sim}{I}$ AS THE OUTPUT.



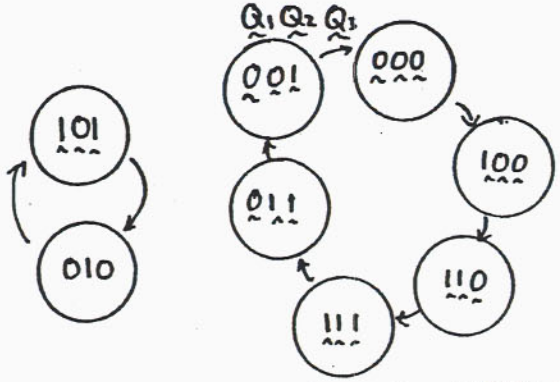
■

12.21 THE LOGIC CIRCUIT IS AS FOLLOWS:



THE THREE RING COUNTERS GIVE AN OUTPUT OF $\underset{\sim}{1}$ AT INTERVALS OF 3, 4 AND 5 CLOCK PULSES RESPECTIVELY. SO $\underset{\sim}{F}$ WOULD BE $\underset{\sim}{1}$ AT AN INTERVAL OF $3 \times 4 \times 5 = 60$ CLOCK PULSES. ALSO THE NUMBER OF FLIP-FLOPS USED = 12. ■

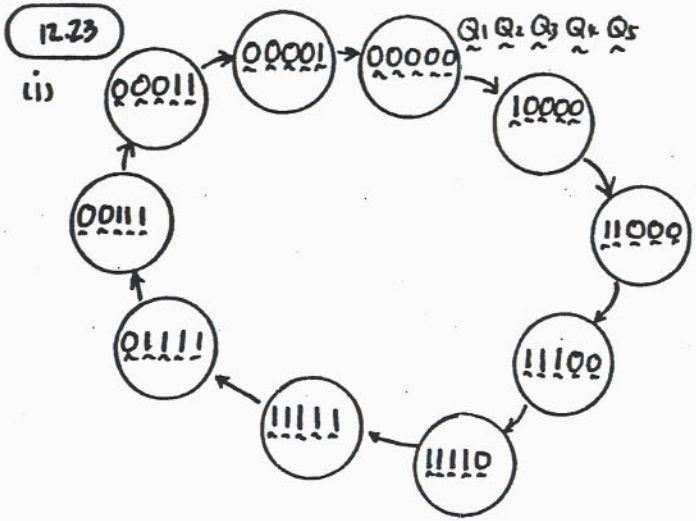
12.22



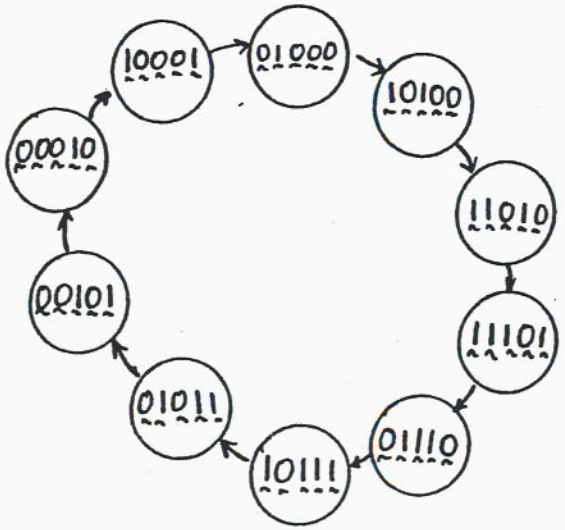
THEREFORE FROM THE STATE DIAGRAM, THERE ARE TWO LIMIT CYCLES.
SINCE THERE ARE 6 STATES IN THE LARGER LIMIT CYCLE, AFTER 6 CLOCK PULSES, THE SYSTEM ALWAYS RETURNS TO ITS ORIGINAL STATE. SO IF WE USE AN AND GATE WITH Q_1, Q_2, Q_3 AS INPUTS, ITS OUTPUT WOULD GIVE A 1 EVERY 6 CLOCK PULSES. THUS WE HAVE A DIVIDE-BY-SIX COUNTER. ■

12.23

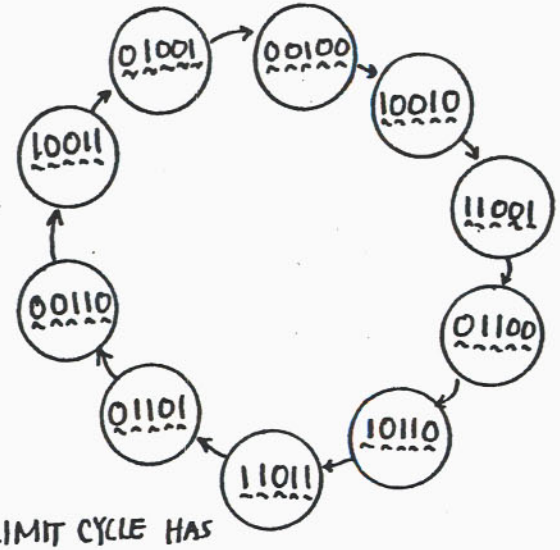
(i)



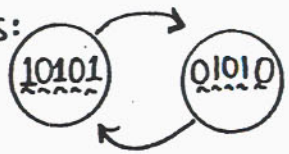
(ii)



(iii)

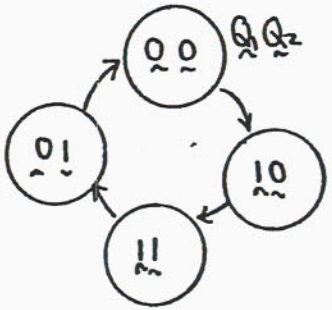


THIS LIMIT CYCLE HAS ONLY 2 STATES:

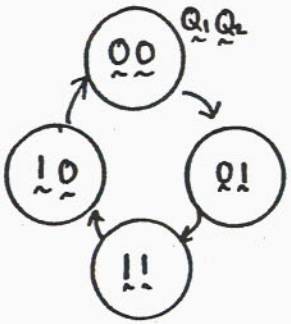


■

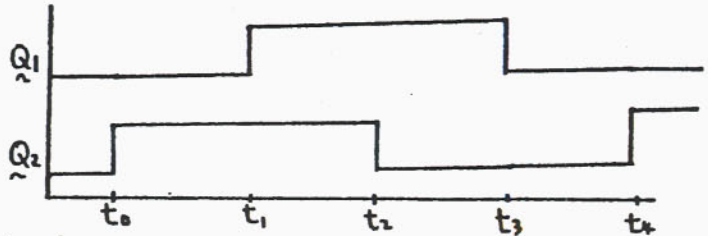
12.24 (a) $A = 1$; $D_1 = \overline{Q_2}$ $D_2 = Q_1$



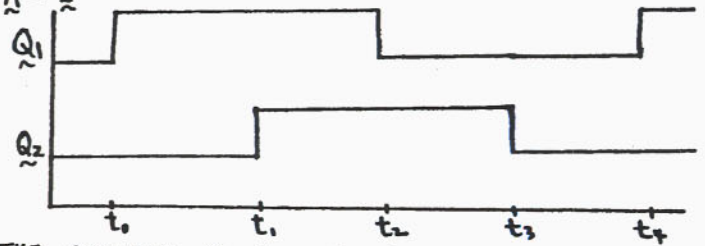
(b) $A = 0$; $D_1 = Q_2$; $D_2 = \overline{Q_2}$



(c) (i) $A = 0$



(ii) $A = 1$



(d) THE OUTPUTS Q_1 AND Q_2 ARE TWO SQUARE WAVES. WHEN $A = 0$, Q_2 LEADS Q_1 IN PHASE BY 90°. WHEN $A = 1$, Q_2 LAGS Q_1 BY 90°. (THE CIRCUIT IS USED TO DRIVE A STEPPING MOTOR – SEE FIG. 17.32. CHANGING A FROM 1 TO 0 REVERSES THE MOTOR. ■