

A. G. Evans
Princeton University,
Materials Institute,
Princeton, NJ 08540
e-mail: anevans@princeton.edu

M. Y. He
Materials Department,
University of California,
Santa Barbara, CA 93106

J. W. Hutchinson
Division of Engineering and Applied Sciences,
Harvard University,
Cambridge, MA 02138

M. Shaw
Rockwell International,
Thousand Oaks, CA 91360

Temperature Distribution in Advanced Power Electronics Systems and the Effect of Phase Change Materials on Temperature Suppression During Power Pulses

A thermal analysis has been performed for a package design pertinent to power electronics. The objective has been the derivation of straightforward expressions that relate the materials used and their physical dimensions to the power input and the junction temperature. This has been done for both steady-state operating conditions and for pulses. The role of phase change materials (PCMs) in suppressing temperature elevations during pulses is also addressed. [DOI: 10.1115/1.1370376]

1 Introduction

For power electronics to be used as motor drives and converters, the preferred packaging approach as well as the design rely on a capability for assuring that the junction temperature be maintained below a maximum: beyond which performance and reliability are compromised. For silicon devices, this temperature is typically, 120°–150C [1–3]. For emerging devices fabricated from wide bandgap materials, such as silicon carbide or gallium nitride, this temperature is above 200C [4]. The specific temperature maximum depends upon the *thermal impedance* of the package, as well as the temporal profile of the power [5]. The temperature elevations that occur during power pulses represent one of the challenges in this arena. While it has been demonstrated that the heat generated by such pulses can be absorbed by introducing *phase-change materials* (PCMs) [6,7], it remains to establish the tradeoff between the enhanced thermal capacity and the decrease in steady-state thermal conductance. One intention of this article is to address this tradeoff by providing straightforward relationships relevant to preliminary design. Detailed designs will still require full-scale numerical analysis. The relationships are developed with reference to a specific packaging approach for an integrated-gate bipolar transistor (IGBT), based on a two-sided design (Fig. 1) that ameliorates the thermal resistance.

Previous thermal analyses provide guidelines [8–11]. General solutions for heat spreading subject to heat transfer boundary conditions have demonstrated the advantages of a dielectric comprising AlN, rather than alumina [8]. These same results identify the preferred thickness of the dielectric and base-plate required for lateral heat diffusion. Other results [9] have demonstrated the highly debilitating influence of an insulating layer (such as a thermal grease) between the base-plate and the heat sink. For the present analysis, it has been assumed that this problem can be obviated by using new heat sink designs [10]. Previous analyses of PCM melting [12–14] have given insight about the materials and layer thickness needed to be effective in this application.

The electronics comprise the power source located near one surface of the chip. The dielectric consists of AlN with a relatively high thermal conductivity, in the range 150–220 W/mK. It has width larger than that for the chip, in order to facilitate heat spreading. PCMs are located between the chip and the AlN. On

the side without the electronics, a metallic PCM is used. On the electronics side, an organic PCM within a metallic open framework is envisaged (Fig. 1(a)). The highly conductive framework helps obviate the inhibition of the temperature suppression caused by the low thermal conductivity of the organic, especially for short power pulses. It also acts as a nucleation site for melting and solidification that inhibits the formation of large shrinkage voids near the interface with the electronics. The AlN is transient liquid phase bonded (TLP) to a Cu heat spreader. However, the results are presented in a generalized form that allows them to be applied to a heat spreader fabricated from Al/SiC (which has a much smaller thermal expansion misfit with the chip than Cu).

The dimensions of the elements comprising the IGBT are given on Fig. 1(a) and the thermal properties are summarized on Fig. 1(b) and Table 1. For initial calibration purposes, interface resistances are neglected, largely because they are unknown for the design depicted on Fig. 1. Since it does not seem useful to guess at these, their effect on the thermal design will be addressed in a subsequent analysis, after preliminary experimental measurements have provided estimates of their magnitudes for the dominant interfaces.

Various thermal boundary conditions are used. In all cases, insulating conditions are imposed at the perimeter. Air-cooling is represented by an effective heat transfer coefficient, h_{eff} , at the surfaces of the base-plate. Water-cooling is simulated by imposing a constant temperature boundary. These two conditions give substantially different temperature distributions and, accordingly, establish differing requirements. Some preliminary numerical calculations demonstrating these differences are presented in Section 3. Thereafter, generalized results for heat transfer boundary conditions are developed.

The objective is to provide straightforward scaling relation that allow preliminary design calculations concerning the sizes of the constituents needed to maximize the power density while maintaining the junction temperature. Basic analytical results are derived that define the general dependencies of the junction temperature on the variables, with coefficients known only in an approximate manner. Numerical results are then generated that both validate the trends and also provide explicit values for the coefficients.

An axisymmetric configuration has been chosen (Fig. 1(a)) with the expectation that this most closely resembles a rectangular IGBT package. That is, the radial heat spreading effects are largely simulated (the extra material in the corner of the rectangle is deemed relatively important). The results will be restricted to

Contributed by the Electronic and Photonic Packaging Division for publication in the JOURNAL OF ELECTRONIC PACKAGING. Manuscript received by the EPPD November 29, 1999; revised manuscript received October 2000. Associate Editor: B. Michel.

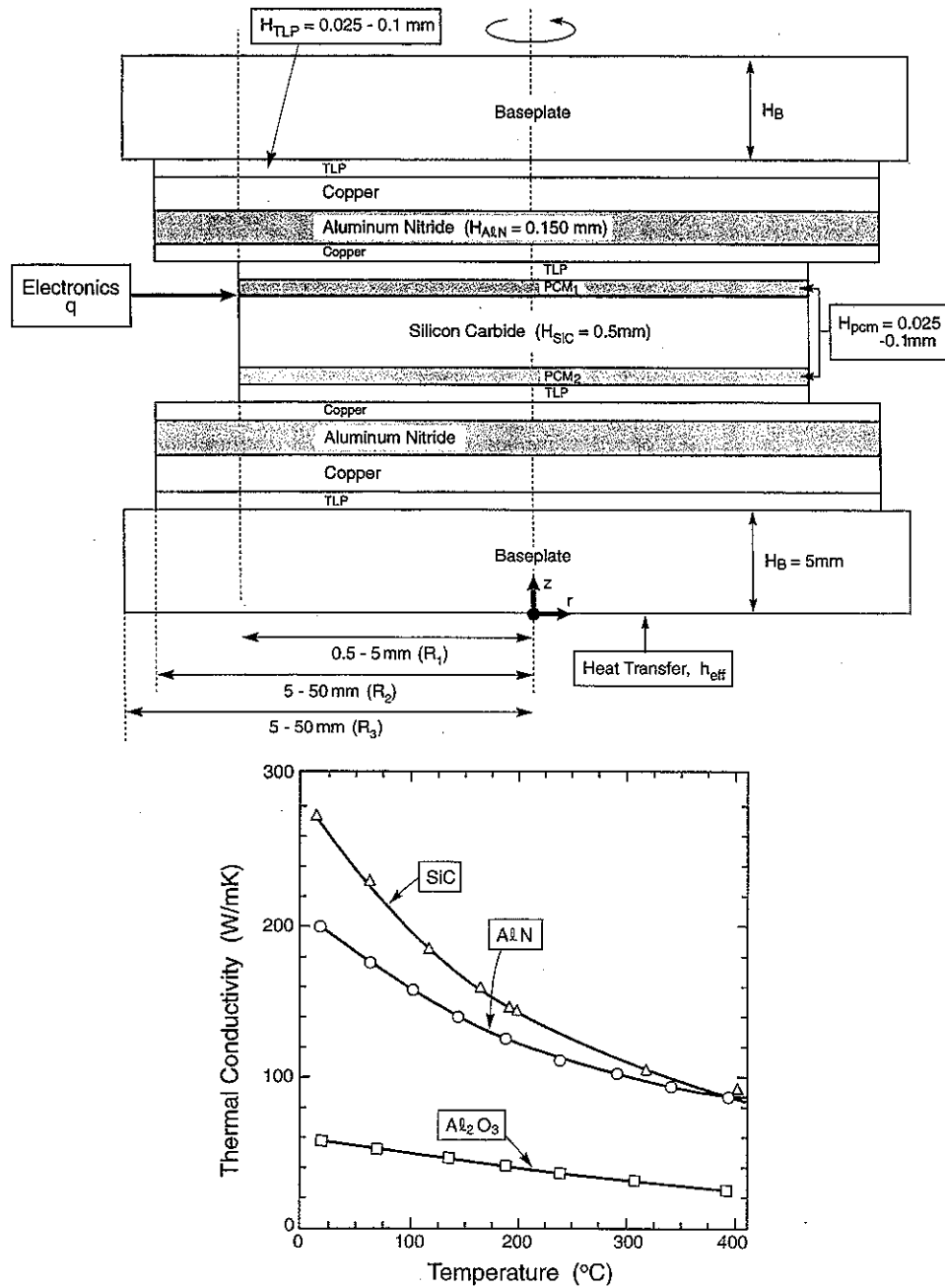


Fig. 1 (a) A schematic of the double-sided configuration: PCM₁ is a metallic and PCM₂ is an organic embedded within a Cu medium. The layers are attached by transient liquid phase bonding (TLP). (b) The thermal conductivities of the constituent materials.

Table 1 Thermal properties

Material	Room temperature Thermal conductivity (W/mK)	Latent heat (kJ/kg)
SiC	400	-
AlN	50-222	-
Cu	400	-
PCM ₁ (metallic)	30-60	300
PCM ₂ (organic)	10-100*	250

*Metal framework used to enhance thermal conductivity.

cases wherein the temperature rise in the fluid coolant is small. For designs that allow the fluid to become relatively hot, a full 3-D simulation becomes essential. Such scenarios are beyond the scope of the present study.

2 Boundary Conditions and Preliminary Results

The package (Fig. 1(a)) has several thermal features inherent to its design, elucidated by performing preliminary numerical calculations that establish key aspects of the temperature distributions. They allow choices for the thermal domains governing the behav-

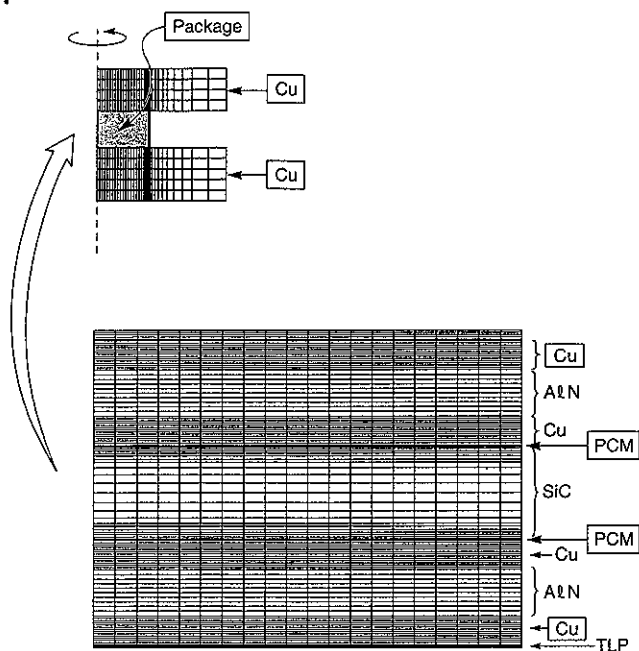


Fig. 2 The finite element mesh used in the calculations

ior. Subject to these findings, approximate analytical formula, are derived, with unknown nondimensional coefficients to be determined by numerical analysis. For the latter, a general-purpose finite element code, ABAQUS, has been used. A typical mesh for the two-sided system has 2090 4-noded linear diffusive heat transfer elements (Fig. 2). The melting of the PCM is simulated by using a temperature-dependent specific heat (Appendix). A power density is imposed at the electronics at time zero and temperatures calculated through the transient to steady-state.

The temperatures that develop in the package are strongly influenced by the boundary conditions used at the base-plate. The effects are illustrated by comparing and contrasting the temperatures that develop at the junction for temperature and heat transfer boundaries. In both cases, the peripheral boundaries are taken to be thermally insulating: a condition most appropriate to a multi-chip configuration. For the former, the temperature, T_o , on the outer boundaries of the base-plates is held constant. Such conditions may be approached when water-cooling is used. For the second, a heat transfer coefficient is used to characterize the heat flowing from the base-plates into a flowing fluid having inlet temperature, T_o , typical of forced air cooling. Once this contrast has been demonstrated, all of the subsequent analysis is performed for heat transfer boundary conditions.

For temperature boundary conditions, the time taken for the system to reach steady-state, after applying the power, is relatively short (several ms) and the steady-state junction temperature, T_j^{ss} , is largely governed by the lowest thermal conductivity constituent, at the appropriate thickness. Noteworthy features pertaining to T_j^{ss} are illustrated on Figs. 3 and 4.

(i) It is increased by the presence of the PCMs, because of their relatively low thermal conductivity. However due to their thinness compared with the other layers, the effects are not significant (Fig. 3).

(ii) It is quite sensitive to the thermal conductivity achievable in the dielectric. Notably, a high grade AlN ($k_{AlN} = 220$ W/mK) reduces T_j^{ss} appreciably relative to a lower grade material ($k_{dielectric} = 50$ W/mK) (Fig. 3).

(iii) The ratio of the radii of the base-plate and chip, R_3/R_1 , has essentially no effect when T_o is prescribed.

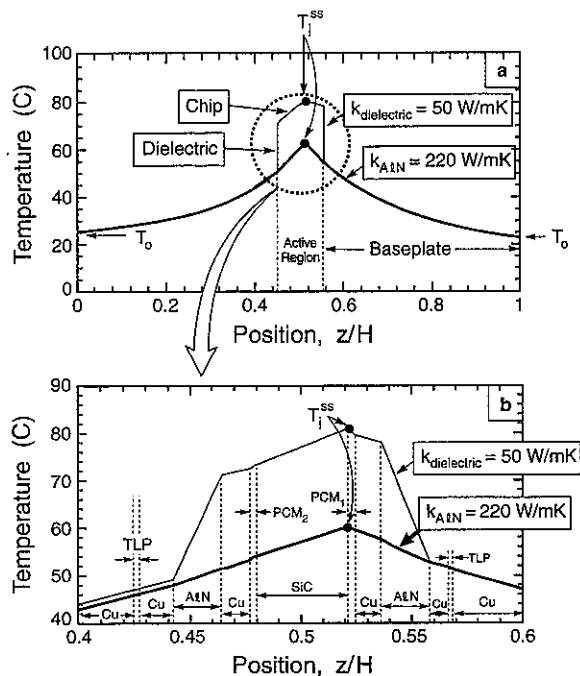


Fig. 3 Axial steady-state temperature distribution for a configuration subject to temperature boundary conditions applicable to water-cooling. Note the appreciable effect of the thermal conductivity of the AlN on the steady-state temperatures.

Heat transfer boundary conditions with air-cooling are different because, for all realistic values of the heat transfer coefficient, there must be an appreciable temperature differential, ΔT , between the surface of the base-plate and the cooling air. This difference is essential for realization of the heat flux into the coolant. This effect causes higher, more uniform axial temperatures (along z). Upon using a representative h_{eff} (100 W/m²K), a preliminary result (Fig. 5) for the configuration depicted on (Fig. 1(a)) illustrates this and other features. For $R_3/R_1 = 40$ and $k_{AlN} = 220$ W/mK, the temperatures along the axis (z at $r = 0$) now vary from 110 C at the junction to 72 C at the base-plate surface (Fig. 5(a)). This profile allows the temperature jump into the coolant ($\Delta T = 47$ C) to be consistent with the imposed power density. For the configuration of Fig. 1(a), the relatively thick base-plate acts as an effective spreader that minimizes the radial gradient (Fig. 4). This finding is used in the analytical derivation described

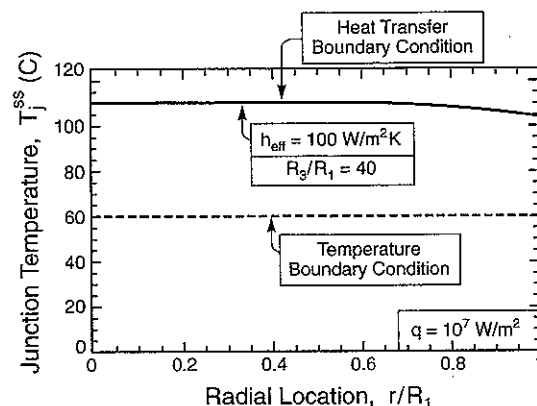


Fig. 4 Radial temperature distributions in the SiC chip for both temperature and heat transfer boundary conditions

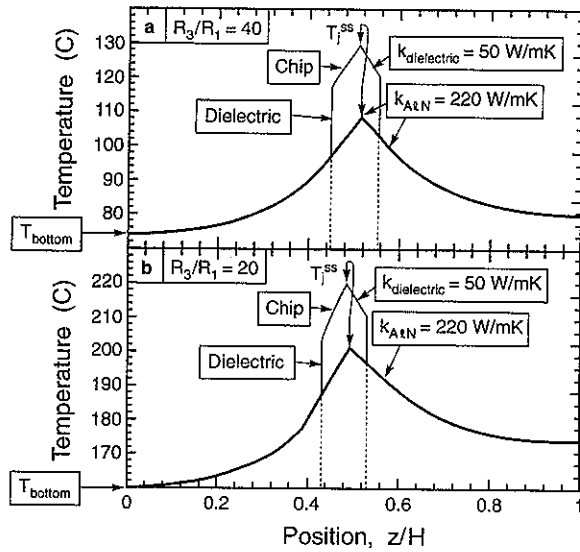


Fig. 5 Axial steady-state temperature distributions for heat transfer boundary conditions appropriate to air cooling: (a) $R_3/R_1=40$, (b) $R_3/R_1=20$

in the next section. Other package designs would admit appreciably larger gradients and could not be approached in the present manner.

In contrast to the behavior found for thermal boundary conditions, the temperatures now depend sensitively on the radius ratio, R_3/R_1 . For example, at smaller R_3/R_1 (20 instead of 40) the temperature differential, ΔT , between the surface of the Cu base-plate and the cooling air is substantially larger ($\Delta T=135$ C) (Fig. 5b). The temperature drop and its dependence on the base-plate size are reflected in the following analytical expressions.

3 Basic Analytical Results

The thermal behavior to be analyzed is shown schematically on Fig. 6. There are three main phases: (1) The junction temperature attained in steady-state, T_j^{ss} , at power density, q_{ss} . (2) The additional transient temperature rise ΔT_{pulse} that develops upon applying a power pulse, Δq . (3) The duration Δt_{melt} of the temperature suppression enabled by PCM melting. The subsequent temperature rise (4) after the liquid front has passed through the PCM is not of interest for a correctly designed system.

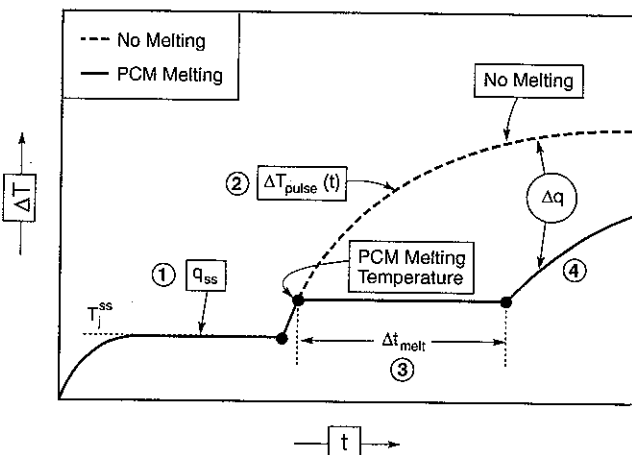


Fig. 6 A schematic showing the four phases subject to analysis

3.1 Heat Diffusion. Before proceeding, an estimate of the heat diffusion distance gives perspectives on the interdependencies of the first two phases: (1) and (2) in Fig. 6. The pulses of interest have on-chip power densities in the range 10^7 to 10^8 W/m² for up to about 1 ms. The distance, z , traversed by the heat pulse, from the electronics plane, after the pulse is applied, is [8]:

$$z \approx \sqrt{\kappa_c t} \quad (1)$$

where κ_c is the thermal diffusivity. Inserting typical diffusivities for the chip and for Cu (Table 1), the distance traveled in 1 ms is about 100 μ m. Accordingly, the heat does not reach the outer surface of the base-plate (5 mm away) before the pulse terminates. The temperature response at the junction is thus unaffected by the thermal conditions at the outer boundaries. The implication is that the steady-state and pulse problem can be addressed separately and the results superimposed.

3.2 Steady-State. For steady-state, two aspects of heat dissipation can be separated: (a) heat transfer from the bottom of the base-plate into the cooling medium, and (b) heat conduction from the junction to the base-plate. Heat transfer for a symmetric, two-sided system can be expressed in term of the average temperature of the fluid, T_o , and that at the bottom of the base-plate, \bar{T}_{bottom} , through the exact result [8],

$$\bar{T}_{bottom} - T_o = (q_{ss}/2h_{eff})(R_1/R_3)^2 \quad (2)$$

The preliminary numerical results (Fig. 4) have indicated that the heat spreading enabled by the base-plate is sufficient to assure that \bar{T}_{bottom} is quite uniform. Hence, for preliminary analysis, the effect of conduction on the temperature through the base-plate can be expressed using [8]:

$$k_{Cu} \partial \Delta T / \partial z \approx q_{ss} \quad (3)$$

which upon integration provides an estimate of the temperature drop across the base-plate along the center-line:

$$\bar{T}_{top} - \bar{T}_{bottom} \cong (q_{ss}/k_{Cu})H_B \quad (4)$$

where \bar{T}_{top} is the temperature at the top of the base plate. Comparison of (4) with (2) using representative values of the parameters reveals that the temperature drop across the base-plate is quite small compared to the temperature difference between the bottom of the base-plate and the cooling medium. The difference in temperature between the electronics and the top of the base-plate is similarly small. It is convenient to express the total temperature drop across the device as

$$\bar{T}_j^{ss} - \bar{T}_{bottom} \cong [(q_{ss}/k_{Cu})H_B] \chi \quad (5)$$

where \bar{T}_j^{ss} is the average temperature at the junction. The gradient coefficient, χ , depends upon the thermal properties of the other constituents in the system (PCM, SiC, TLP), which must be determined numerically. Combining (2) and (5) gives the nondimensional result:

$$\tau_{ss} \cong [(\bar{T}_j^{ss} - T_o)(h_{eff}/q_{ss})] = [(R_1/R_3)^2 + \chi Bi] \quad (6)$$

with Bi being the Biot number [8]:

$$Bi \cong h_{eff}H_{Cu}/k_{Cu}$$

Expression (6) will be tested numerically and the coefficient χ determined.

The utility of (6) is governed largely by the relative invariance of χ . Namely, if χ depends weakly on q_{ss} and H_B , as well as R_1/R_3 and R_2/R_3 , it can be used to establish scaling effects with minimal numerical analysis.

3.3 Transient Temperatures. During the power surge, a proportion α of the pulse power, Δq , flows into the PMC adjacent to the junction, and the remainder $((1-\alpha)\Delta q)$ flows into the chip. The partitioning factor α is given by [8]

$$\alpha = \left[1 + \frac{k_{SiC} \sqrt{\kappa_{PCM}}}{k_{PCM} \sqrt{\kappa_{SiC}}} \right]^{-1} \quad (7)$$

This relation is valid during the transient, before melting of the PCM, and before the interfaces above the PCM and below the chip begin to influence the temperature pulse. Equation (7) is obtained by solving the thermal diffusion equation for the temperature increase, ΔT , above and below the electronics junction plane ($z=0$) [8]:

$$\frac{\partial^2 \Delta T}{\partial z^2} = \frac{1}{\kappa} \frac{\partial \Delta T}{\partial t} \quad (\kappa = \kappa_{PCM} \text{ for } z > 0; \kappa = \kappa_{SiC} \text{ for } z < 0) \quad (8a)$$

subject to the three conditions

$$k_{PCM} \frac{\partial \Delta T(0^+, t)}{\partial z} = -\alpha \Delta q, \quad k_{SiC} \frac{\partial \Delta T(0^-, t)}{\partial z} = (1-\alpha) \Delta q, \quad \Delta T(0^+, t) = \Delta T(0^-, t) \quad (8b)$$

The solution to this boundary value problem is:

$$\Delta T(z, t) = \frac{\alpha \Delta q \sqrt{\kappa_{PCM} t}}{k_{PCM}} f(\xi) \text{ for } z > 0 \text{ where } \xi = z^2 / (\kappa_{PCM} t)$$

$$\Delta T(z, t) = \frac{(1-\alpha) \Delta q \sqrt{\kappa_{SiC} t}}{k_{SiC}} f(\xi) \text{ for } z < 0$$

where $\xi = z^2 / (\kappa_{SiC} t)$ (8c)

The function $f(\xi)$ satisfies a second order ordinary differential equation on the interval $0 < \xi < \infty$. This function will not be detailed here. The primary value of interest is $f(0) = 2/\sqrt{\pi}$ [9]. This value provides the transient temperature rise at the electronics junction plane due to the power surge:

$$\Delta T(0, t) = \frac{\alpha \Delta q \sqrt{\kappa_{PCM} t}}{k_{PCM}} f(0) \quad (9)$$

As emphasized, this solution provides the temperature rise for times less than those at which the neighboring layers become affected by the pulse. For presenting numerical simulations, (9) motivates the introduction of a nondimensional temperature increase due to the surge as

$$\Delta \tau \equiv \Delta T(0, t) k_{PCM} / (\Delta q \sqrt{\kappa_{PCM} t}) \quad (10)$$

When the conditions for validity of (9) pertain, $\Delta \tau \equiv \alpha f(0)$.

Numerical calculations are used below to determine the relative constancy of $\Delta \tau$ for typical pulses. Again, provided that the deviations from constancy are small, (10) establishes the predominant scaling.

3.4 PCM Melting. It is anticipated that, upon PCM melting, the junction temperature will remain relatively constant and equal to the PCM melting temperature T_m until the melt front extends through the PCM, at time Δt_{melt} . This assertion will be validated below by numerical analysis. For pulses longer than Δt_{melt} , T_j will begin to rise rapidly (Fig. 6).

If all of the power from the pulse were consumed in PCM melting, the transient would be [8]

$$\Delta t_{melt}^* = (L\rho H)_{PCM} / \Delta q \quad (11a)$$

where L is the latent heat per unit mass, ρ the density and H_{PCM} the thickness of the PCM. The actual time should exceed this, through a proportionality, b ,

$$\Delta t_{melt} = b \Delta t_{melt}^* \quad (11b)$$

This proportionality is related to the partitioning coefficient, α , indicative of the fraction of the heat entering the PCM. It is of order:

$$b \approx (1-\alpha)^{-1} \quad (11c)$$

By evaluating b numerically and determining its deviation from unity, its merit as a characterizing parameter for the melting transient will be established.

4 Numerical Results

4.1 Steady-State. It is apparent from (5) that the trends in steady-state are most effectively expressed by exploring the coefficient, χ , for various designs. Accordingly, the numerical results for the steady-state junction temperature are plotted using the ordinate:

$$\chi = [\tau_{ss} - (R_1/R_3)^2] / Bi \quad (12)$$

Results for a full range of heat transfer coefficients (10 to 200 W/m²K) and constituent thermal conductivity, as well as a large range in size ratio, R_3/R_1 , are plotted in this manner on Fig. 7. It is apparent that χ is relatively invariant with heat transfer coefficient, as well as the power density (in the ranges studied), but varies somewhat with the thermal conductivity of the dielectric; changing from 6 to 8×10^{-6} as $k_{dielectric}$ changes from 220 to 50 W/mK. Because of its constancy, the utility of χ for scaling purposes is validated.

4.2 Transient Temperatures. Calculations absent PCM melting (Fig. 8(a)) indicate that the temperature transient is, indeed, independent of the heat transfer coefficient. The role of the partitioning coefficient, α (7), is illustrated by comparing the thermal transient for Si and SiC chips (Fig. 8(b)). The higher thermal conductivity of the SiC, relative to Si, reduces α by about 30%. This reduction is reflected in the correspondingly lower temperature, $\Delta T(t)$, shown on Fig. 8(b), as anticipated by (9).

All other calculations are conducted for SiC. The results are replotted with $\Delta \tau$ (10) as the ordinate (Fig. 9) and time as the abscissa. It is apparent that, except at short times (≈ 1 ms), $\Delta \tau$ is time-invariant. The nonconstancy at very small times almost certainly reflects numerical error, rather than a deviation from (10), as evident from a few calculations performed with a shorter time step.

The numerical results reveal that there is an influence of the pulse amplitude, Δq , on $\Delta \tau$. However, the effect is quite small: $\Delta \tau$ increases by less than a factor 2 for a two order of magnitude increase in Δq . The behavior arises because of the temperature dependence of the thermal conductivity of SiC has been accounted for in the numerical simulation, which causes α to vary as the pulse amplitude changes.

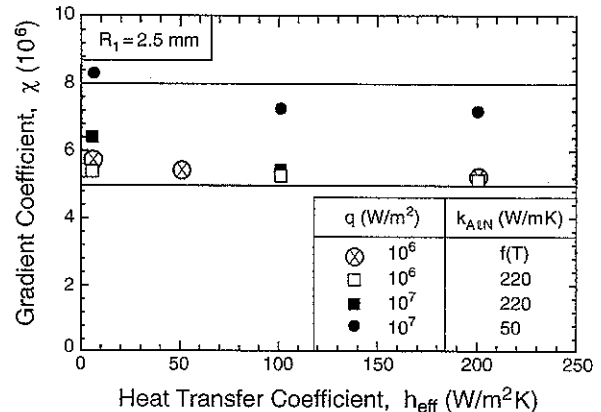


Fig. 7 The magnitude of the gradient coefficient, χ , for a range of system variables

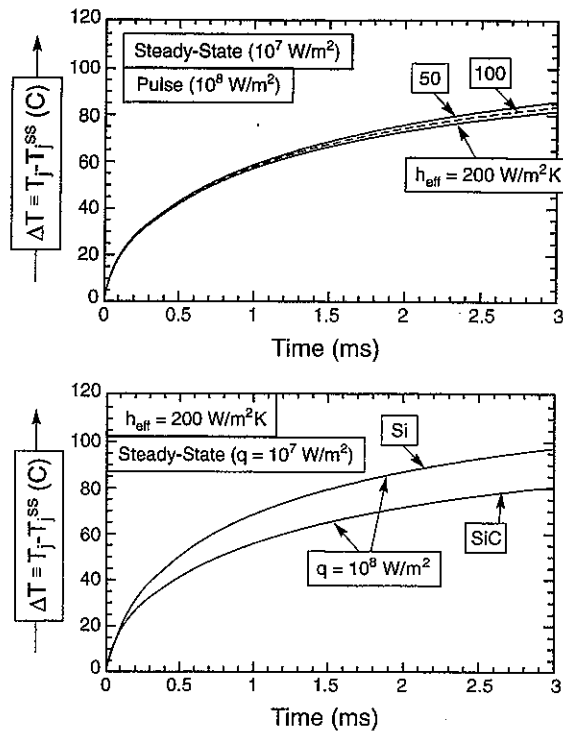


Fig. 8 Transient temperatures, without PCM melting, calculated for typical pulses; (a) effect of heat transfer coefficient, (b) effect of chip thermal conductivity

4.3 Melting Times. Illustrative calculations incorporating PCM melting are presented on Fig. 10(a). As anticipated by (11), thermal damping is strongly influenced by the PCM thickness. To explore this transient, the non-dimensional parameter b (11b) is plotted against PCM thickness (Fig. 10(b)). It is relatively constant and has magnitude, $b \approx 1.5$. It is larger than unity because of the partitioning of the heat between the PCM and the chip (7). Accordingly, (11a) may be used with this b to estimate Δt_{melt} and to obtain the PCM thickness and thereby, to design the thickness of the PCM to assure that it does not fully melt before the pulse has been switched off. For example, using the parameter set indicated on Table 1, with $\Delta q = 10^8 \text{ W/m}^2$ and a 1 ms pulse, then for a metallic PCM, it would be required that $H_{PCM} \approx 120 \mu\text{m}$. This thickness would increase in almost direct proportion with the pulse amplitude. For organic PCMs, even though L per unit mass

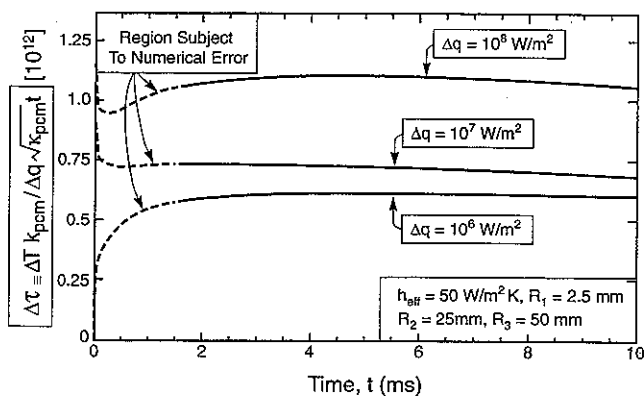


Fig. 9 The variation in the nondimensional temperature, $\Delta\tau$ (10), with time (absent PCM melting) for three different pulse magnitudes

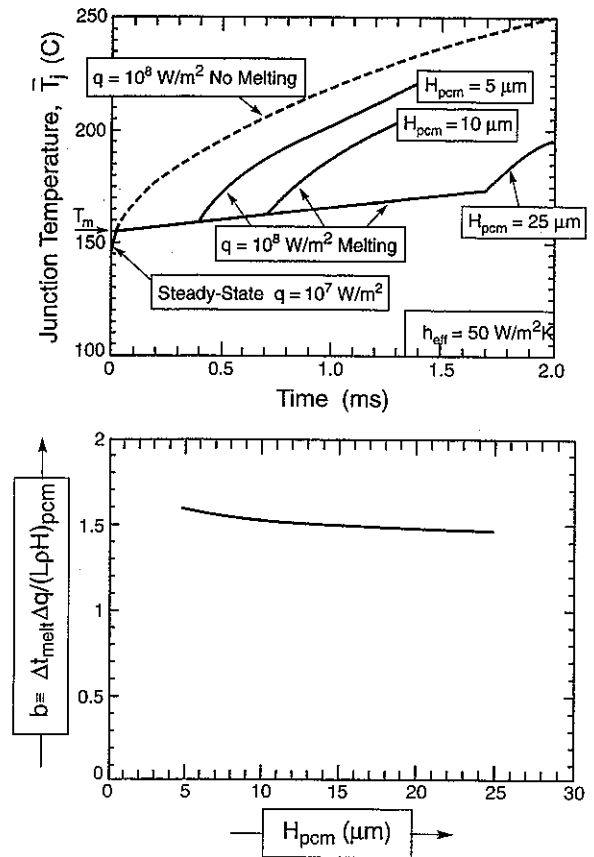


Fig. 10 (a) Transient temperatures upon PCM melting calculated for three PCM thicknesses. (b) The magnitude of the time coefficient, b , and its dependence on PCM thickness.

can be about the same as that for the metallics, their lower density requires that the PCM layer be substantially thicker.

5 Implications for Package Design

5.1 Steady-State Temperatures. An initial design goal that can be readily addressed using (5), with the above numerical values for χ , concerns the compactness of the system, manifest in its minimum overall volume:

$$V_{\min} \approx 2\pi H_B R_3^2 \quad (13a)$$

which with (5) becomes:

$$V_{\min} = \frac{2/h_{eff}}{[T_j^{ss}/PH_B - \chi/\pi k_{Cu} R_1^2]} \quad (13b)$$

where P is the power on the chip

$$P = \pi R_1^2 q \quad (13c)$$

Here $2H_B$ represents the overall thickness of the package.

This result can be interpreted in several ways.

(i) There is an inverse linear dependence of the volume on the heat transfer coefficient. That is, increasing h_{eff} has a major influence on compactness.

(ii) Changing from Si to SiC electronics to increase T_j^{ss} also reduces the package size. However, the impact depends on other aspects of the design. The maximum possible effect is inverse linear: wherein the factor 3 increase in T_j^{ss} achieved with SiC (relative to Si) reduces the volume by 1/3.

(iii) As the power requirements increase, the system volume must increase. The increase in overall volume could be ameliorated by increasing the chip diameter $2R_1$.

Another perspective is gained by rearranging (5) to express trends in the power:

$$P = \frac{T_j^{ss}/H_B}{1/\pi H_B R_3^2 h_{eff} + \chi/\pi k_{Cu} R_1^2} \quad (14)$$

The important implication is that, for fixed overall volume, enhancements in the power capabilities depend linearly on the junction temperature, such that SiC electronics are preferable to Si. Also, larger chip size, R_1 , allows P to be increased, but the details are design dependent.

5.2 Transients. The behavior following a pulse can be assessed by combining the results from (10) and (11b) and noting that, $\kappa = k/\rho c_p$, with c_p being the specific heat. The most important parameter is the total time taken to melt the PCM, t_{melt} , given by:

$$t_{melt} = \left(\frac{\rho_{PCM}}{\Delta q} \right) \left\{ \frac{(k c_p)_{PCM} (T_m - T_j^{ss})^2}{\Delta \tau^2} + b(LH)_{PCM} \right\} \quad (15)$$

where T_M is the PCM melting temperature. By setting t_{melt} to be less than the pulse time, the peak junction temperature is limited to about T_M . Accordingly, (15) may be used to design the package using $\Delta \tau$ from (13) and b from Fig. 10(b).

5.3 Other Considerations. The absence of interface resistances in the calculations and in the formulas are clearly a limitation. These can be readily introduced once realistic values for this package have been estimated by experimental measurements. It is hoped that, because transient liquid phase (TLP) bonding is used, that the resistances would be small. However, within the PCM layer, upon melting and resolidification, some shrinkage porosity might develop, resulting in an appreciable degradation. It is hoped that this effect would be minimized by using the metal framework, which should act as a nucleation site for solidification. This remains to be determined.

6 Conclusion

For the power package design depicted on Fig. 1(a) it has been possible to derive straightforward expressions for the junction temperature that can be used to establish guidelines for designing compact systems. The expressions involve three coefficients to be determined numerically: χ , $\Delta \tau$, and b . Results obtained for a full range of heat transfer coefficients and for a wide range of material properties relevant to this package, have established that these three coefficients are nearly invariant. Accordingly, they may be used as constants for preliminary design and sizing of the package. Subject to these preliminary designs, full numerical calculations would be needed to converge on a final design.

For most of the designs envisaged, the entire system would operate at temperatures within a few tens of degrees of the junction temperature itself. This would have the added benefit that the residual stresses at steady-state operation are reduced, compared to a package that operates subject to a large temperature gradient. This favorable situation arises because the stress-free temperature, that at which the package has been fabricated (by transient liquid phase bonding), is above the junction temperature.

Appendix

Numerical Modeling of Melting. Most of the codes available for analyzing thermo-mechanical problems such as

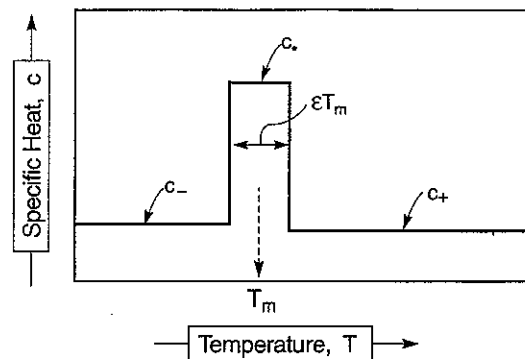


Fig. 11

ABAQUS cannot directly model the propagation of a melting front. However, the codes do accommodate a temperature dependent specific heat, and it is possible to employ this dependence to account for the latent heat of melting. To this end, let c denote the volume specific heat (in J/m^3K) of the PCM with c_- its value prior to melting and c_+ in the liquid state. Consider the temperature dependence of c shown in Fig. 11 where T_m is the melting temperature and the elevated value within a very small temperature interval, εT_m , centered on the melting temperature is:

$$c_* = \frac{1}{\varepsilon T_m} + \frac{1}{2}(c_- + c_+) \quad (A1)$$

The term $(c_- + c_+)/2$ in c_* ensures that the heat absorbed per unit volume as the temperature increases from below $(1 - \varepsilon)T_m$ to above $(1 + \varepsilon)T_m$ is exactly, $c_-(T_m - T_1) + c_+(T_2 - T_m) + L$. Thus, a temperature dependent specific heat can account for heat absorbed by melting. The finite temperature interval (εT_m) during which the elevated specific heat operates must be chosen to be sufficiently small that the errors incurred are small relative to the predictions for a material with a distinct melting temperature. However, the smaller εT_m , the smaller must be the time step used in the numerical simulation. There are additional implications for the spatial meshing in the PCM, but these are less restrictive than the limitations on the time step.

References

- [1] ASM Electronics Materials Handbook, 1986, Volume 1, *Packaging*, ASM International.
- [2] Taraseiskey, H., 1996, *Power Hybrid Circuit Design and Manufacture*, Marcel Dekker, Inc.
- [3] Sze, S. M., 1981, *Physics of Semiconductor Devices*, Wiley, NY.
- [4] McCluskey, F. P., 1997, *High Temperature Electronics*, CRC Press.
- [5] Tummala, R. R., and Rymaszewski, E. J., 1989, *Microelectronics Packaging Handbook*, Van Nostrand Reinhold.
- [6] NASA CR-61363, 1971, *Phase-Change Materials Handbook*.
- [7] NASA Technical Paper 1074, "A Design Handbook for Phase Change Thermal Control and Energy Storage Devices."
- [8] Lu, T. J., Evans, A. G., and Hutchinson, J. W., 1998, *ASME J. Electron. Packag.*, **120**, pp. 280-289.
- [9] Van Vodbold, C., Sankaran, V. A., and Hudgins, J. L., 1997, *IEEE Trans. On Power Electronics*, **12**, pp. 3.
- [10] Lu, T. J., Stone, H. A., and Ashby, M. F., 1998, *Acta Mater.*, **46**, pp. 3619-3635.
- [11] Neugebauer, C. A., Yerman, A. F., Carlson, R. O., Burgess, J. F., Webster, H. F., and Glascock, J. H., 1986, *The Packaging of Power Semiconductor Devices*, Gordon and Breach, NY.
- [12] Lu, T. J., 2000, *Int. J. Heat Mass Transf.*, **43**, pp. 2245-2256.
- [13] Laouadi, A., and Lacroix, M., 1999, *Int. J. Heat Mass Transf.*, **42**, pp. 275-286.
- [14] Muehlbauer, J. C., and Sunderland, J. E., 1965, *Appl. Mech. Rev.*, **18**, pp. 951-957.